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Implementation Of A Low Power Dissipation And Area Efficient Decoder Using Mixed Circuit Logic

D.A. Tatajee(Asst.professor) , V. Amal Prathyusha, D. Rama Harika, V. Sai Sowjanya and P. Kusumakumari
Department Of Electronics and Communication Engineering
Vignan's Institute Of Engineering For Women, Visakhapatnam

Abstract- This paper briefly presents a review on VLSI line decoders by using different logic types such as complementary metal oxide semi-conductor(CMOS), transmission gate logic(TGL), pass transistor dual value logic(PDVL) and mixed circuit logic. A comparison of these techniques are represented based on their performance such as propagation delay, power dissipation and area. In order to analyze these different logic styles, a 2-to-4 decoder is considered. Simulations are done on this decoder in different logic styles as mentioned above using Mentor Graphics software. Based on the observation and analysis of the circuits, it is conveyed that CMOS logic is more robust at low power supply, TGL provides full swing in output for specific inputs, PDVL design has fast restoration capability with moderate speed and power dissipation and mixed logic provides the advantages of CMOS, TGL and PDVL. It also provides low power dissipation and area efficiency.

Keywords-; CMOS; Mixed circuit logic; TGL; PDVL; VLSI line decoders.

I. INTRODUCTION

The performance of VLSI circuits are impacted by the significance of each logic style. These circuits are designed by aiming few factors such as reduction of power dissipation, propagation delay and to provide area optimization. Most of the battery powered applications deal with these methods to prolong the life of the battery. Such applications can be designed by using CMOS logic styles which dissipates less power. CMOS design has equal number of n-type and p-type MOSFETs. CMOS logic exhibits high input impedance. It is used to design universal gates such as NAND and NOR. To obtain the output of basic gates an additional inverter is required.

This drawback can be overcomed by using TGL. A TGL gate is designed by parallely connecting the source and drain terminals of a pair of n-type and p-type MOSFETs. TGLs are bidirectional so the inputs can be applied to either of the short circuited terminals. The AND/OR logic are realized easily and effectively by using double pass transistor compared to CMOS logic. Adapting transmission gate logic which improves full swing output and noise margin. The drawback in TGL is that it does not provide faster restoration in output for specific inputs. Third alternative logic is PDVL, it provides full swing and faster restoration charge at output. The switching speed is also improved because it consists a single path for charging and separate path for discharging. PDVL requires less number of MOS devices compared to other logic styles. Fourth alternative method is mixed circuit logic where it combines the advantages of the other three logic styles, reduces the power dissipation, propagation delay and area.

For comparison of these logic styles, the abstraction level that is transistor level is best suited so a 2-4 decoder is designed in this level.

II. CMOS LOGIC STYLE

A 2-4 line decoder has 2 inputs and 4 outputs. In order to design an AHO decoder we need to design a NOR gate where the AHO decoder produces the output high and the others are low. These type of decoders are used in the construction of multiplexers. In order to design an ALO decoder we need to design a NAND gate where it produces the low output and the others are high. A CMOS logic produces the inverted output so we can design universal gates such as NAND and NOR gates. An AHO decoder is considered. A CMOS circuit consists of PMOS as the pull up network and NMOS as the pull down network. CMOS logic style provides high input impedance because the input is given to the gate terminals of the MOSFETs.

MOSFETs acts as a switch in all logic types. If logic '1' is given as an input to the nMOS then it acts as a closed switch and it is considered as ON whereas for the same given input the pMOS acts as the open switch and its status is OFF. If logic '0' is given as an input to the pMOS then it acts as a closed switch and the status is considered as ON whereas for the same input the nMOS acts as an open switch and the status is considered as OFF. A decoder is designed with inputs A, B and outputs Y0, Y1, Y2 and Y3.

Advantages of CMOS logic style are low static power dissipation and it is sustainable for changes in supply voltages. This logic style is independent of transistor sizing and it has high noise margin. CMOS logic is a ratio less logic, but the aspect ratio between the p-MOS and n-MOS must be maintained. Even though the supply voltage is reduced the CMOS design produces the allowable output levels. The layout design of the CMOS designs is simple and compact. More compactness is attained at the time of fabrication, during fabrication the p-MOS is placed in the n-well where the p-MOS and n-MOS devices are separated by a demarcation line. Device count is high in CMOS logic compared to the other

logics. CMOS designs have less driving capability. In order to boost the voltage level near to the supply voltage, and additional inverters or buffers are used.

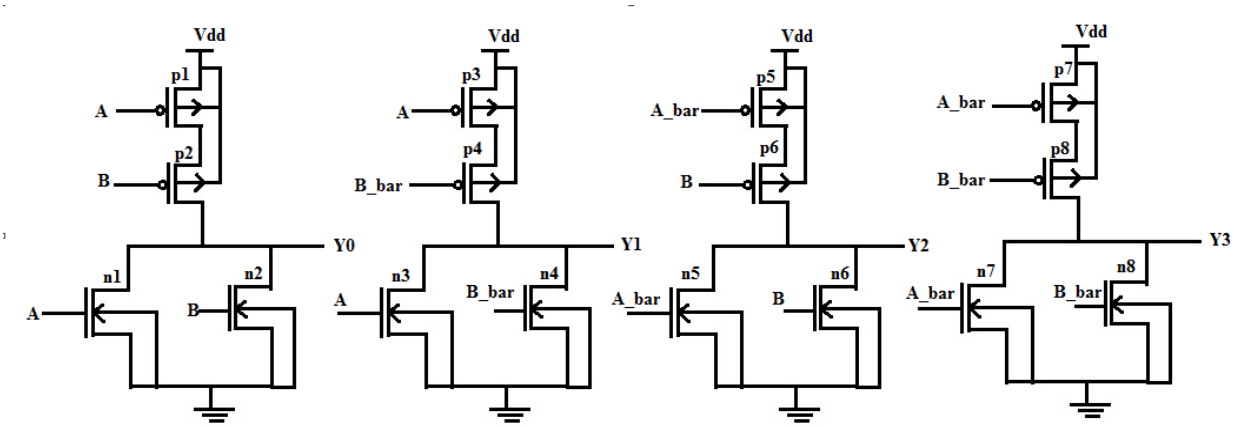

FIG 1: 2-4 DECODER IN CMOS LOGIC STYLE

inputs	Status of n-MOSFETs and p-MOSFETs	outputs

A	B	N1	N2	P1	P2	N3	N4	P3	P4	N5	N6	P5	P6	N7	N8	P7	P8	Y0	Y1	Y2	Y3
0	0	off	off	on	on	off	on	on	off	on	off	off	on	on	on	off	off	1	0	0	0
0	1	off	on	on	off	off	off	on	on	on	on	off	off	on	off	off	on	0	1	0	0
1	0	on	off	off	on	on	on	off	off	off	off	on	on	off	on	on	off	0	0	1	0
1	1	on	on	off	off	on	off	off	on	off	on	on	off	off	off	on	on	0	0	0	1

TABLE 1: FUNCTION TABLE OF CMOS 2-4 DECODER

III. TRANSMISSION GATE LOGIC

Transmission gate is the combination of a p-MOS and n-MOS device connected in parallel where the source and drain of these devices are short circuited and the input is applied at either of the two short circuited ends. The switching action of the transmission gate can be controlled by using the gate terminals of n-MOS and p-MOS. The main advantage of this logic type is that it can produce strong '0' and strong '1' that means it provides a full swing output at the output node. The main concerns are as follows:

- TGL requires less number of transistors compared to conventional CMOS logic.
- Non-inverting AND/OR gates can be realized easily.
- Pre-charge is done through the p-MOS and then it discharges through the n-MOS, thus the switching speed is improved.
- Drawback in TGL is that it cannot provide expected voltage restoration for specific input combinations.

TGL circuit of 2-4 decoder:

The circuit of TGL 2-4 decoder is shown in fig-2. An AHO decoder is designed by using AND gates at the output. To design an AND gate an n-MOS device and a TG gate is required. The input is applied is through the TGs and the output transition occurs only when the n-MOS is ON. A 2-4 TGL decoder is realized by using four TGs and four n-MOS. Complimented inputs are given to the devices. Discharging path is separately incorporated in order to improve the switching speed. The aspect ratios of the MOSFETs should be maintained properly to maintain full swing output. The transistor sizes of n-MOS and p-MOS are one-third and two-third compared to pass transistor logic. The speed of TG gates is high compared to CMOS.

IV. PASS TRANSISTOR DUAL VALUE LOGIC

The improvements over double pass transistor implements a pass transistor dual value logic by discarding the redundant branches. A single MOS device is used as the pull-up network. So, the aspect ratio of the pull-up network must be carefully chosen to provide balance with the pull down network. PDVL can be referred as a ratio logic. The width as well as the length

values should be maintained fixed in order to obtain equal rise time, fall time and restoration capability.

- It maintains good speed in spite of using single MOS device in the pull-up network.
- Reduced device count and full swing in output is observed compared to other two logic styles
- Redundant branches are removed at the nodes and transition at nodes are eliminated.

PDVL circuit of 2-4 decoder:

A 2-4 decoder is designed by using a PDVL logic is shown in fig 3. Two inputs are given to the gate and drain terminals of the p-MOS device which is in the pull up network. If input A=0, B=0 then the output Y0=1 because p1 is on where n1 and n2 will be off, the same is performed for other input combinations and recorded in a table. An AHO decoder is designed by using AND gate. To design an AND gate a p-MOS is placed in the pull-up network and two n-MOS devices are placed in the pull down network. In order to design an ALO decoder an OR gate is required, in order to design an OR gate two p-MOS devices are used in the pull up network and a single n-MOS is used in the pull down network. The PDVL logic style has moderate speed and power dissipation compared to the CMOS and TGL logic. The supply voltage is given to the pull-up p-MOS network and the inputs are given to the gate and source terminals. The source terminals of pull down n-MOSs are connected to the ground. The aspect ratio of single p-MOS in the pull up network is balanced with the ratio of all n-MOS in the pull down network. All the input combinations produce strong '0' and strong '1'.

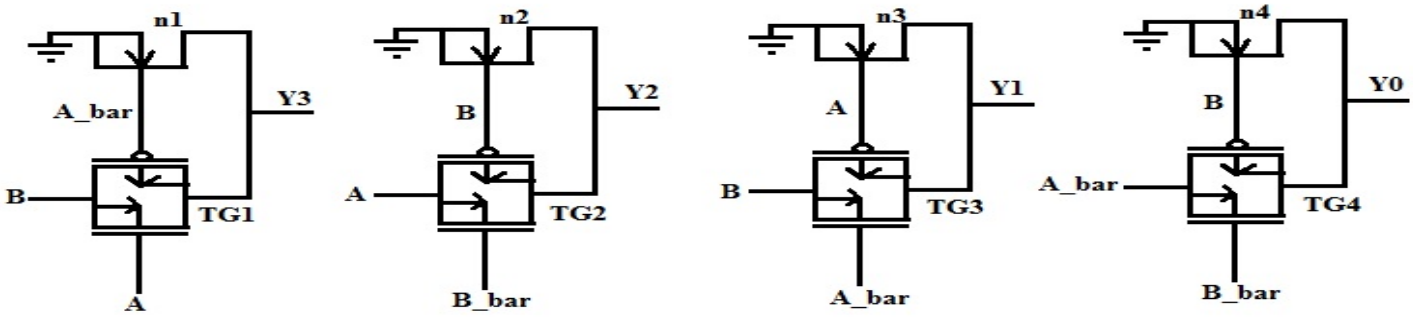

FIG 2: A 2-4 DECODER USING TGL

inputs	Status of transmission gates and n-MOSFETs	outputs

A	B	TG1	N1	TG2	N2	TG3	N3	TG4	N4	Y0	Y1	Y2	Y3
0	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	OFF	ON	OFF	ON	0	1	0	0
1	0	ON	OFF	OFF	ON	ON	OFF	ON	OFF	0	0	1	0
1	1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	0	0	0	1

TABLE 2: FUNCTION TABLE OF TGL BASED 2-4 DECODER

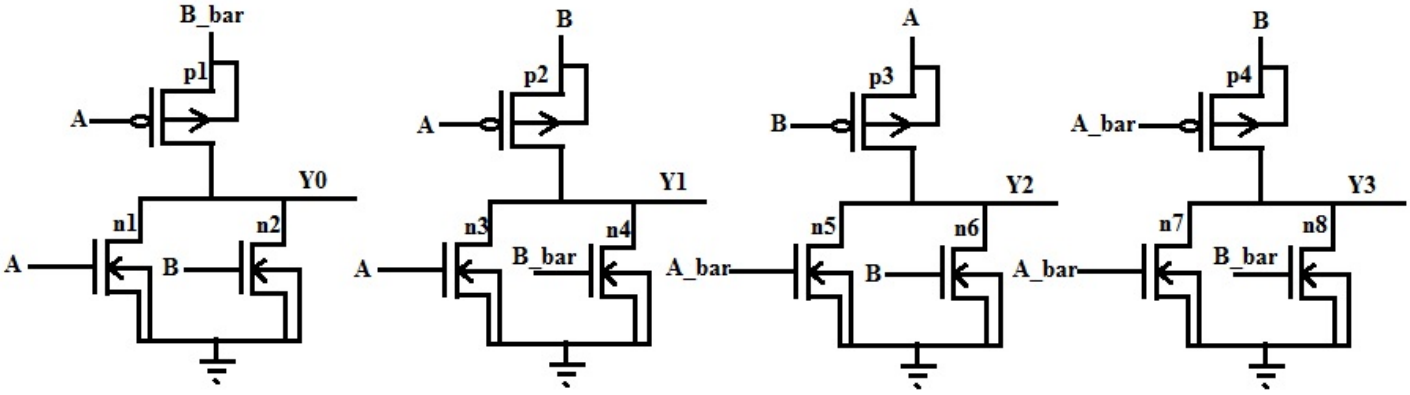

FIG 3: 2-4 DECODER USING PDVL

Inputs	Status of n-MOSFETs and p-MOSFETs	outputs

A	B	N1	N2	P1	N3	N4	P2	N5	N6	P3	N7	N8	P4	Y0	Y1	Y2	Y3
0	0	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	0	1	0	0
1	0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	0	0	1	0
1	1	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	0	0	0	1

TABLE 3: FUNCTION TABLE OF PDVL BASED 2-4 DECODER

V. MIXED CIRCUIT LOGIC

The mixed circuit logic combines the CMOS, TGL and PDVL techniques in order to achieve low operating power, low power dissipation, minimal die area and high performance. In this proposed design a 2-4 decoder can be designed by using 14 transistors, that is D0 and D2 are the AND gates using pass transistor dual value logic, where D1 and D3 are the AND gates using Transmission gate logic and an inverter is also considered . Fig 4 shows the mixed logic design to realize 2-4 decoder. Advantages of mixed circuit logic

- It provides full swing output and full restoration capability.
- Redundant branches are removed.
- Low power dissipation, minimal area and low operating output.

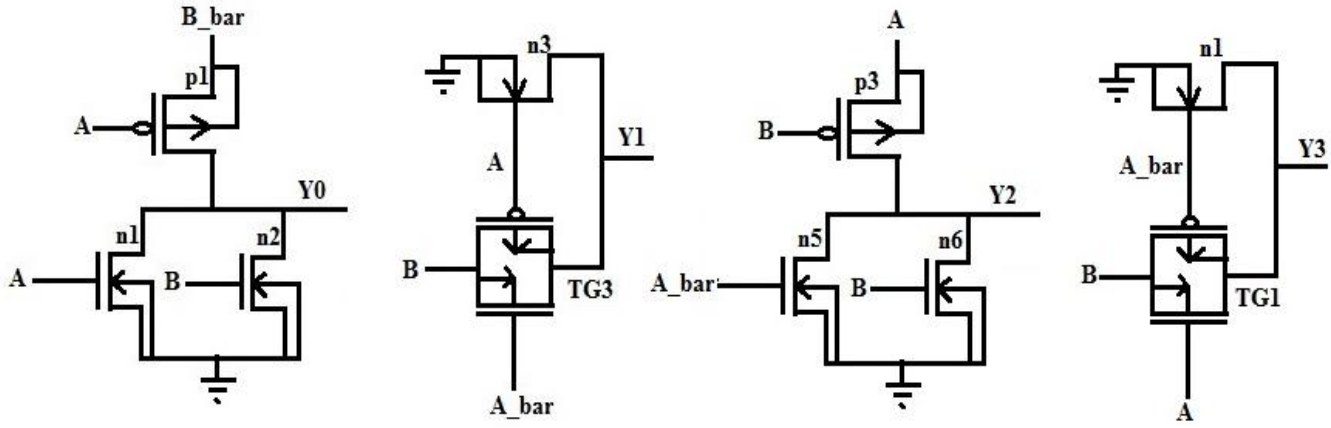

FIG 4: 2-4 DECODER USING MIXED CIRCUIT LOGIC

inputs	Status of n-MOS, p-MOS and TGs	outputs

A	B	N1	N2	P1	N3	TG1	N4	N5	P2	N6	TG2	D0	D1	D2	D3
0	0	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	ON	ON	ON	OFF	ON	OFF	0	1	0	0
1	0	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	0	0	1	0
1	1	ON	ON	OFF	ON	OFF	OFF	ON	ON	OFF	ON	0	0	0	1

TABLE 4: FUNCTION TABLE OF 2-4 DECODER USING MIXED CIRCUIT LOGIC

VI. IMPLEMENTATION AND RESULT

The implementation of a 2-4 decoder is designed in four different logic styles. These circuits are developed and verified by using mentor graphics130nm technology, the schematics of 2-4 decoders using different logic styles such as CMOS, TGL, PDVL and mixed circuit logic is shown in fig 5, fig 6, fig 7 and fig 8. A decoder in four different styles is simulated. The power dissipation is proportional to the square of the supply voltage and frequency of transitions. The inputs A and B are at maximum voltage i.e. at supply voltage and the minimum value is zero. The power dissipation, propagation delay that are obtained for different logic styles is shown in table 5, table 6. The area of the designs is calculated in terms of number of transistors used by the design for different logic styles is shown in table 7. The output waveforms are also shown in the figures below.

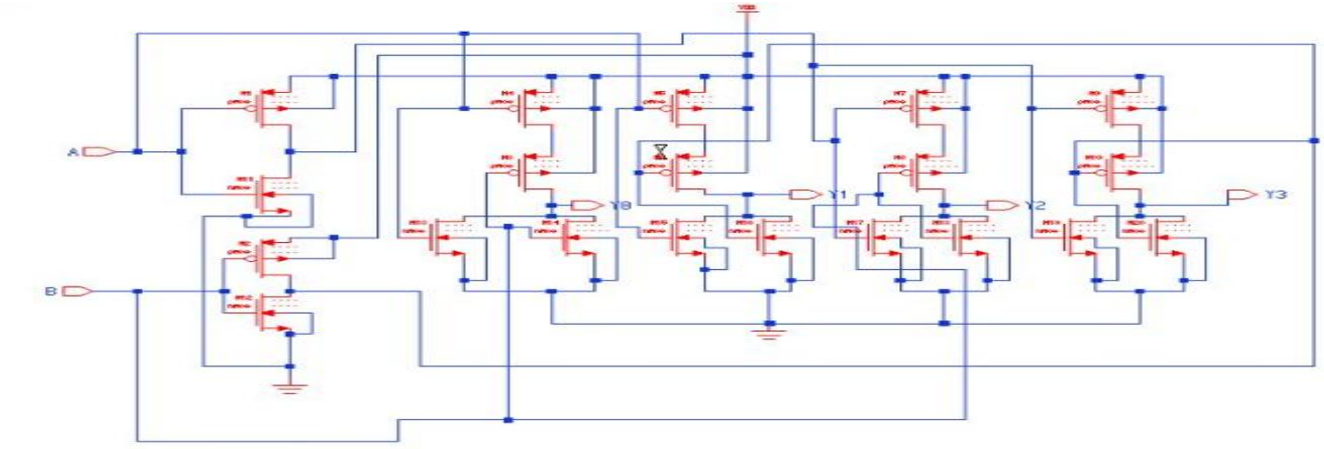

FIG 5: SCHEMATIC DIAGRAM OF CMOS 2-4 DECODER

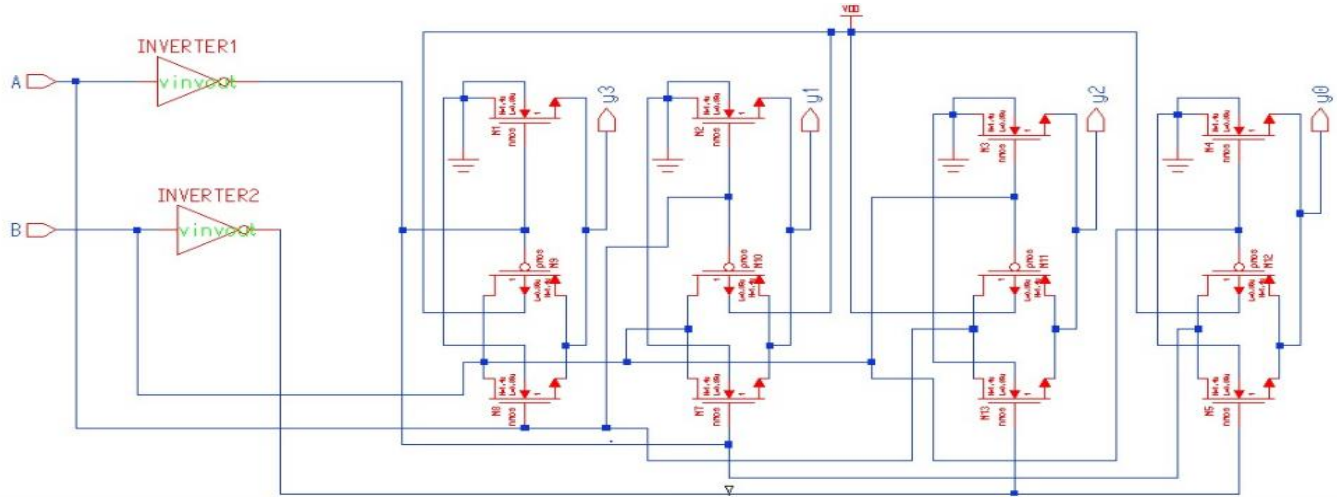

FIG 6: SCHEMATIC DIAGRAM OF TGL 2-4 DECODER

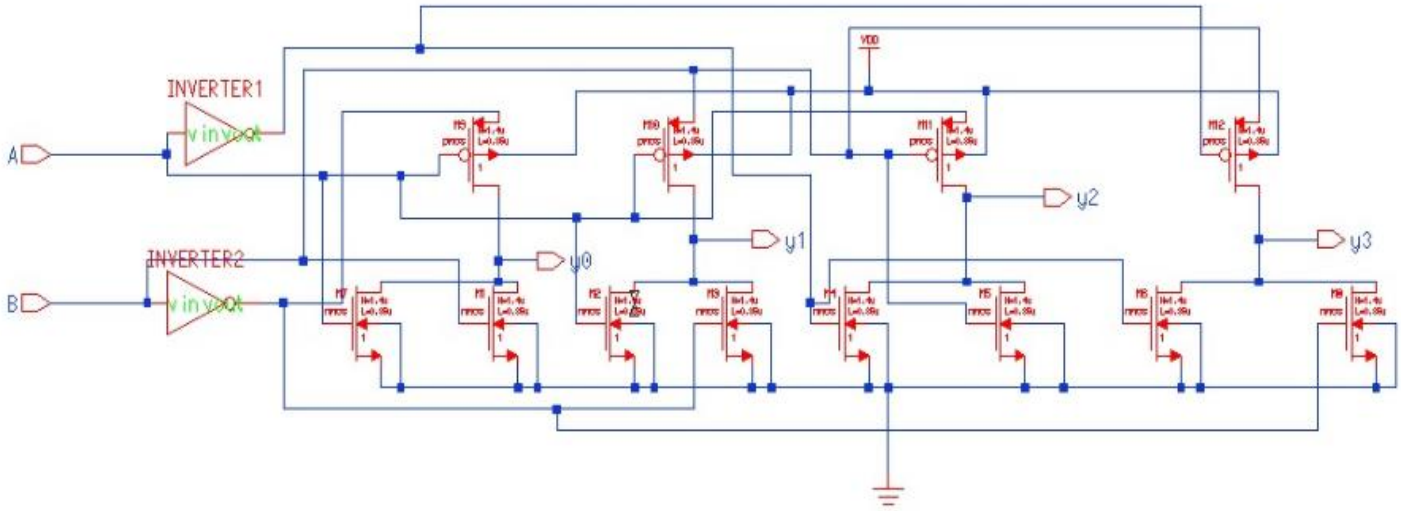

FIG 7: SCHEMATIC DIAGRAM OF PDVL 2-4 DECODER

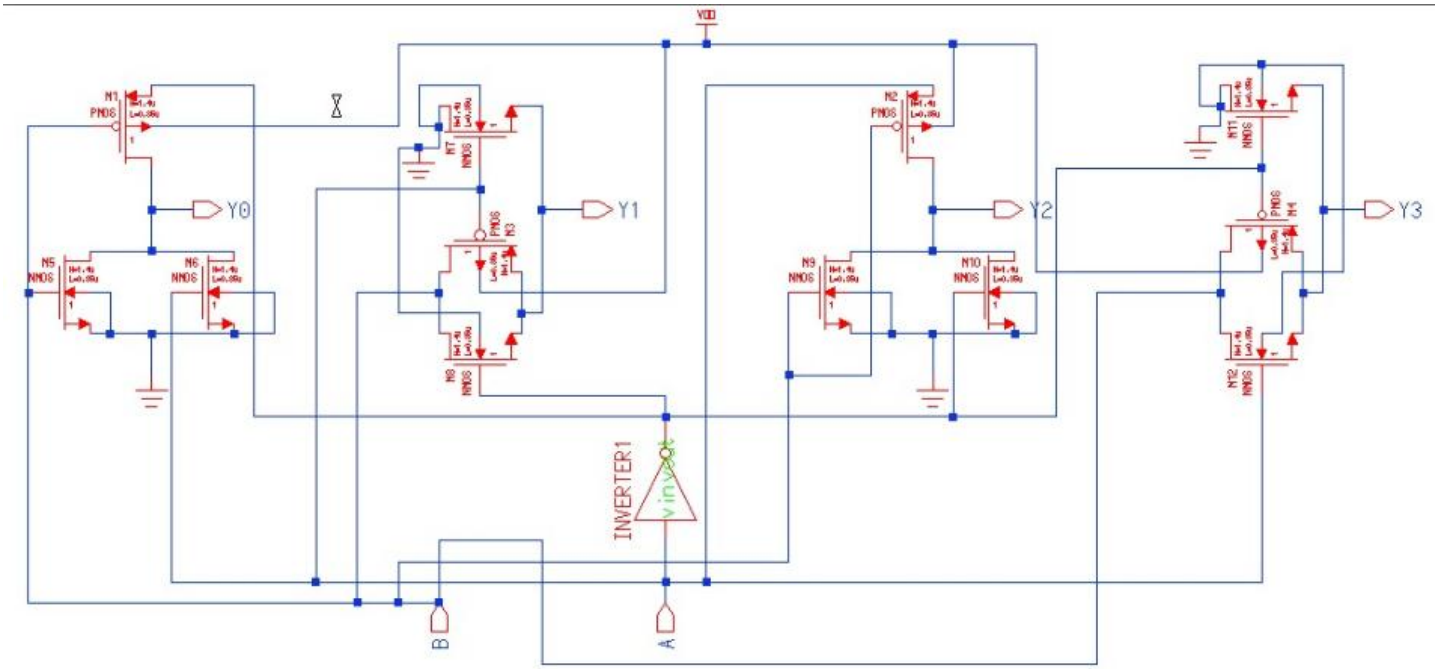

FIG 8: SCHEMATIC DIAGRAM OF MIXED CIRCUIT 2-4 DECODER

TABLE 5: TOTAL POWER DISSIPATION OF A 2-4 DECODER

LOGIC STYLE	5V
CMOS	12.2005nw
TGL	6.8452nw
PDVL	9.0102nw
MIXED CIRCUIT	6.7952nw

TABLE 6: PROPAGATION DELAY (NS) OF A 2-4 DECODER

LOGIC STYLE	5V
CMOS	149.97
TGL	100.32
PDVL	73.460
MIXED CIRCUIT	50.006

TABLE 7: AREA EFFICIENCY (NO. OF TRANSISTORS)

Logic style	p-MOS	n-MOS	TGs	Total
CMOS	10	10	-	20
TGL	2	6	4	16
PDVL	6	10	-	16
MIXED CIRCUIT	3	7	2	14

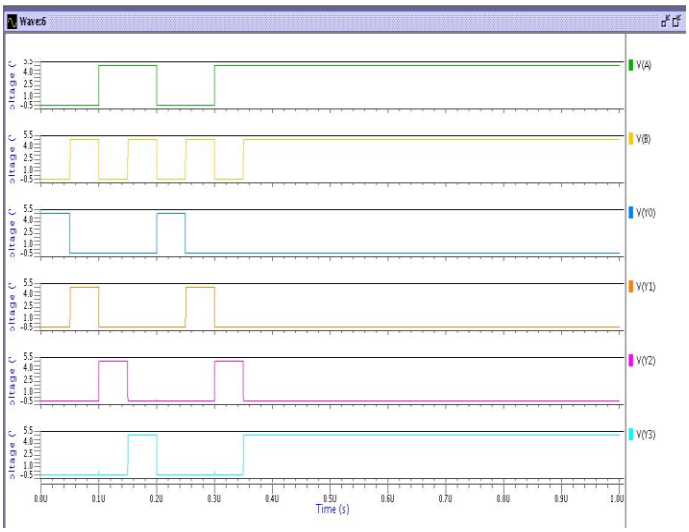

FIG 9: OUTPUT WAVEFORM OF A CMOS 2-4 DECODER

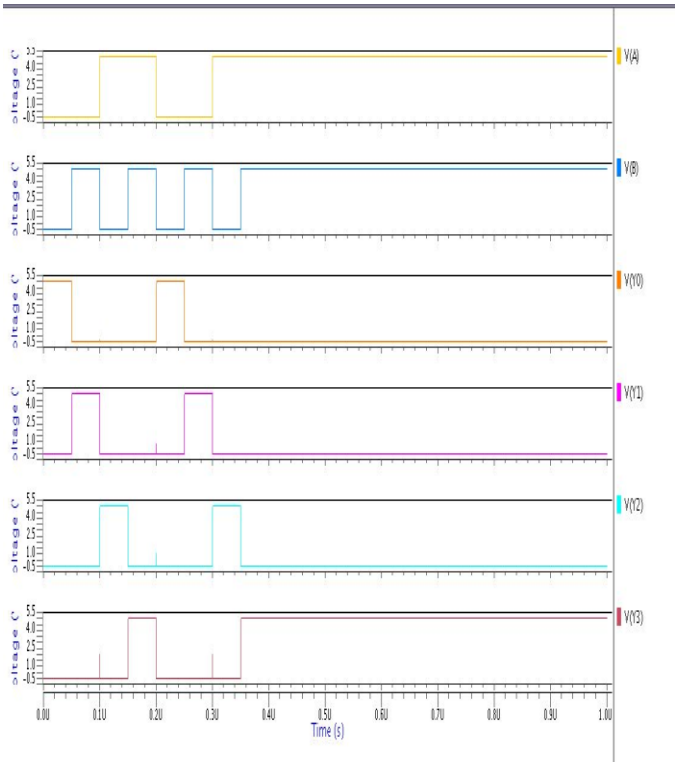

FIG 10: OUTPUT WAVEFORM OF A TGL 2-4 DECODER

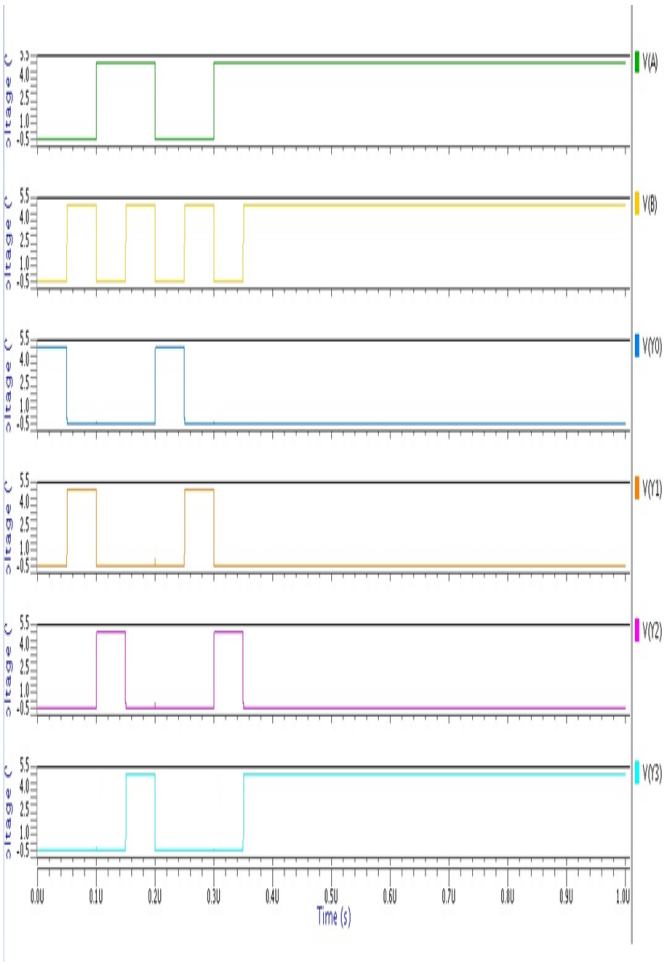

FIG 11: OUTPUT WAVEFORM OF A PDVL 2-4 DECODER

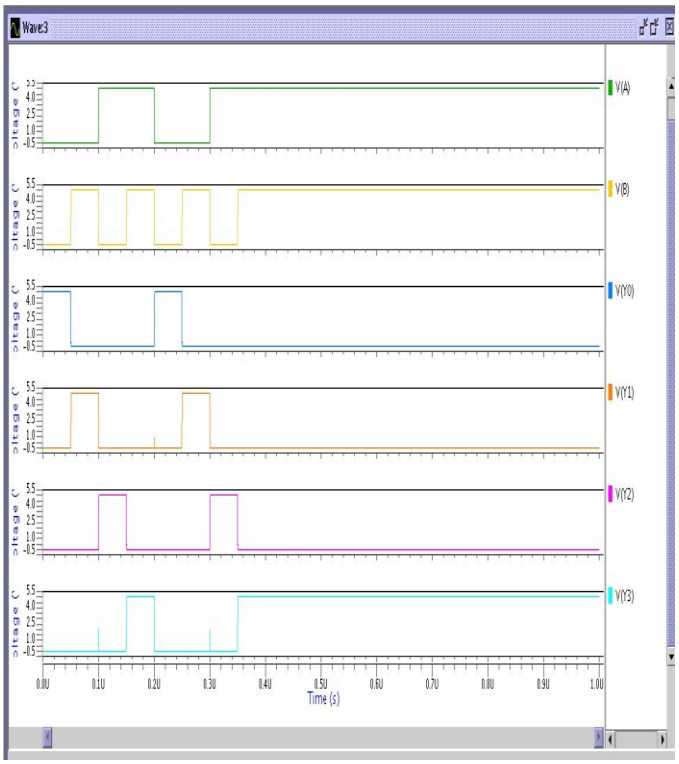

FIG 12: OUTPUT WAVEFORM OF A MIXED CIRCUIT 2-4 DECODER

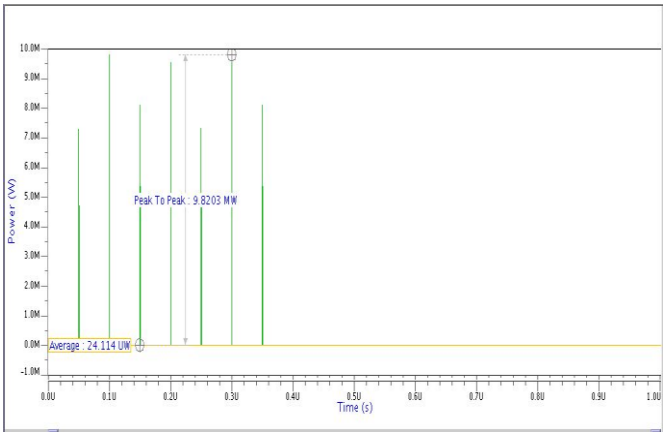

FIG 13: POWER DISSIPATION OF TGL 2-4 DECODER

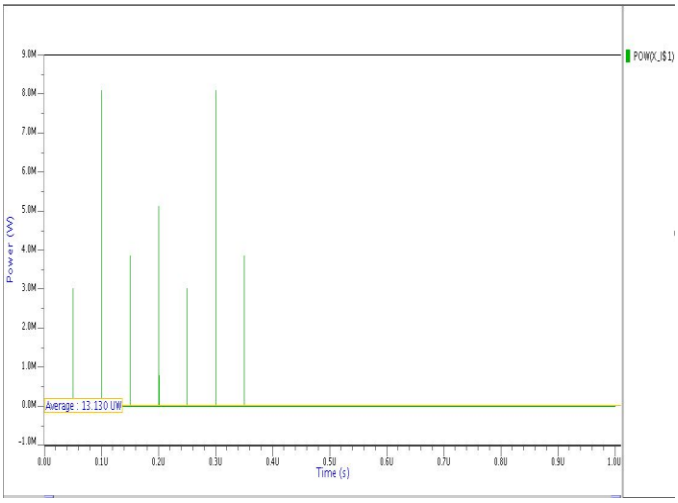

FIG 14: POWER DISSIPATION OF A MIXED CIRCUIT 2-4 DECODER

VII. CONCLUSION AND FUTURE SCOPE

CMOS gives an efficient mixed logic design which is used for decoding circuits. By using above techniques we have a new topology namely as 2–4 low power decoder By using the above techniques which reduces the number of transistors, decreases delay, power and increases the performance of the circuit than compared to the conventional CMOS decoders, TGL and PDVL. By using mixed logic 2:4 decoders as pre decoding circuits in conjunction with CMOS logic. These all technologies provide smart driving capability. The economical low power decoders are designed and enforced in mentor graphics 130nm technology. .The decoders are implemented in mixed logic reduces the facility consumption by 50% and delay by 60% in comparison to standard CMOS decoder. By using physical layout higher output decoders can be implemented, where these decoders can be used as audio signal decoder at receiver end to decode the audio signal. Memory address decoders can also be designed. Generally, these types of decoders used in communication systems like

telecommunications, networking and transfer of data from one end to another end.

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