Power Efficient Shift Register Using Leakage Control NMOS Transistor

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Abstract- VLSI is a stream of electronics engineering which involves putting millions and billions of transistors logically together on to a single chip. VLSI circuits play a vital role in modern digitalized world. FLIP-FLOPS (FFs) are the fundamental storage elements used in digital system designs, which constitutes registers, shift registers, counters etc. The powerdissipation of the FFs employed in a typical digital design has a great influence on its performance. This paperpresentsthe design of a SISO (Serial In Serial Out) register using LCNT(Leakage Control NMOS Transistor) based D Flip Flop. The functional verification is done in mentor graphics tool. The obtained results matching with the expected ones and the comparative analysis with the previous design techniques shows that thiswill be an effective solution for the future low power register designs.

Keyword: LCNT, SISO

I INTRODUCTION

In today's electronics world, there is a drastic change in the size of devices. This led to the development of VLSI technology. It allows as design of circuitswith less power, portability and mobility, with less cost and less environmental effects. FLIP-FLOPS (FFs) are the fundamental storage elements in digital system designs and they find applications in registers, shift registers, counter etc. The 20% - 45% of the total system power is from these basic storage elements. Therefore while designing registers, counters etc. the power dissipation of a flip flop is the major performance limiting constraint. In a classic design model the major limitation of flip flops in VLSI designs is power consumption, power dissipation, delay, clock skew etc. On concern with limitation power dissipation is one of the important constraints which reduce the speed of the device, reliability etc. Our motive is to reduce the power dissipation using different low power techniques. Using these flip flops we would like to design shift registers.

Shift registers are widely used in large number of sequential circuits and processors for temporary storage of data. A shift register is cascade of flip flop, sharing the same clock, in which the output of each flip flop is connected to data input of next flip flop in chain. Serial in Serial Out (SISO) shift register accepts data serially, one bit at a time at the single input line, and shifted to next flip flop serially. The output is also obtained on a single output line in a same serial fashion.

Now-a-days, with the increasing use of mobile devices, laptops, consumer electronics demand a stringent constraint on reducing power dissipation. Flip flops are the key elements used in sequential digital systems. Flip flops and latches are the basic elements for the storing information. Flip flop is one of the most power consumption components. Flip flop can be implementedin different ways. Lector and LCNT techniques increase the efficiency of the design. Using Lector and LCNT the main attention has to decrease power dissipation and increase the performance. There are two types of D flip flops that are found in literature that is single edge triggered and double edge triggered. But the double edge triggered Flip flop suffers from performance degradation, because it samples data on both clock edges. These single edge triggered Flip flops are simple in design and sample data only one clock edge. These are mostly designed by using master slave configuration.The limitation of conventional D flip flop based 4 bit SISO register is its performance characteristics such as power dissipation, efficiency etc. This project presents design of 4 bit SISO using LCNT technique in order to overcome the limitation of conventional design.

II SHIFT REGISTERS:

The Shift Register is a type of sequential logic circuit that can be used for the storage or the transfer of binary data. Shift Register is a cascade of flip flops, sharing the same clock, in which the output of each flip flop is connected to the data input of the next flip flop, resulting in a circuit that shifts by one position(as shown in figure1 and 2) .

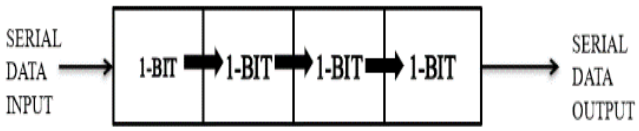

Figure1: Data transfer from left to right using shift register

CLOCK	T0	T1	T2	T3	T4	T5	T6	T7
SERIAL INPUT	1	0	1	1				
Q1		1	0	1	1			
Q2			1	0	1	1		
Q3				1	0	1	1	
Q4					1	0	1	1

Figure 2: Operation of 4-Bit SISO Shift Register

4-BIT SHIFT REGISTERS USING CONVENTIONAL D-FLIP FLOP:

The schematic of 4-bit shift registers using conventional D-flip flop is as shown in figure 3 where conventional D-Flip Flops are connected in cascaded form with one input and one clock.

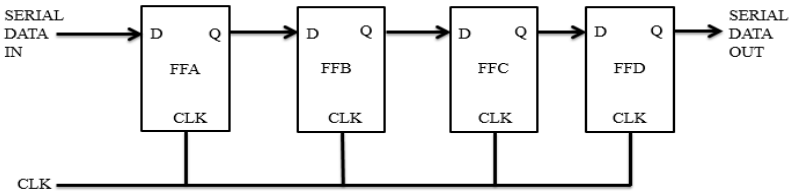

Figure 3: Schematic of 4-Bit Shift Registers Using Conventional D-Flip Flop

IMPLEMENTATION OF CONVENTIONAL D FLIP FLOP

In conventional D flip flop there are two clock signals one is positive clock and other is negative clock. There are pull up and pull down networks. The conventional D flip flop is designed using master and slave networks. The output of the master is given to the slave as input, and also the output of the master is directly connected to the slave output. The main intention is to minimizing the power dissipation. The logic diagram and the schematic of a conventional D flip flop is shown in below figure 4 and 5.

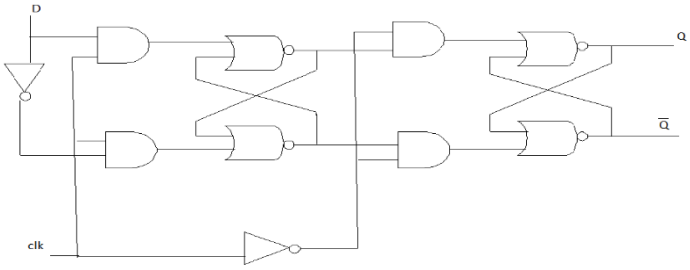

Figure 4: Conventional D-Flip Flop

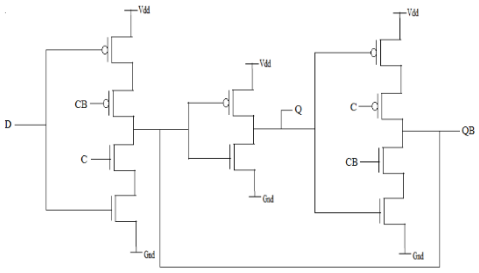

Figure 5: Schematic conventional D-Flip Flop

The conventional D flip flop circuit uses the double gated clock for both master and slave parts of the circuit. The circuitry of gated clocks gives out complements of master and slave.

When the output remains same even though the input or clock changes power gets dissipated irrespective of the output was constant and didn't change.

LECTOR BASED D-FLIP FLOP

Lector is a method to decrease the problem of leakage in CMOS circuits, it includes two extra leakage control transistors, which are self-controlled, in the pathway from supply to ground which offers the extra resistance which will reduce the problem of leakage current in the CMOS circuit.The lector implemented circuits have less power consumption as compared to conventional circuit design. When compared to conventional circuit, lector technique gives low static power dissipation. The Schematic of Lector based D flip flop is shown in figure 6.

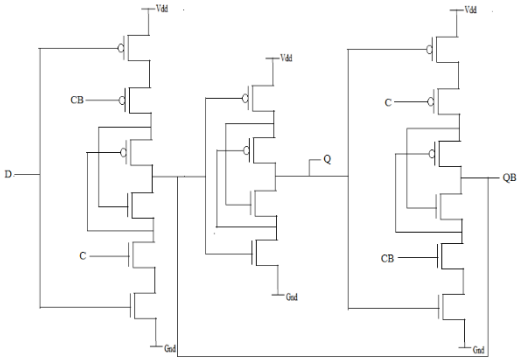

Figure 6: Schematic of Lector Based D-Flip Flop

III. PROPOSED 4-BIT SHIFT REGISTERS USING LCNT BASED D-FLIP FLOP

While comparing different design approaches for the D flip flop LCNT based design gives better efficiency in terms of power dissipation. LCNT is a novel transistor level approach for the minimization of leakage current. This technique implements, two LCTs within a standard CMOS logic circuit. The LCNT Based circuits minimize the leakage power. The LCNT based D flip flop is shown in figure 7.

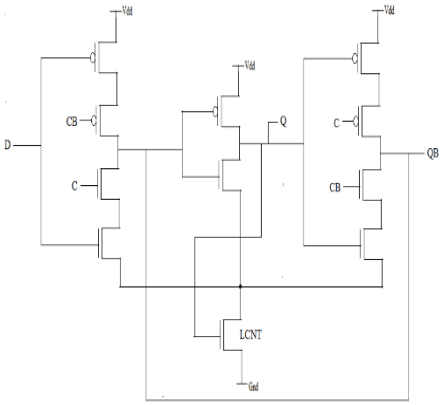

Figure 7: Schematic of LCNT Based D-Flip Flop

When the LCNT is employed in the circuit, only the inverter of the circuit gets affected and the rest of the circuit remains unchanged. After the changes the power dissipation get reduced. The only difference between the lector and LCNT is that is utilize n-channel MOSFET's, which provide an increased path resistance and reduce the current flowing through it and thereby reducing the power consumed.Theproposed 4 bit shift register using LCNT based flip flop is shown in figure 8.

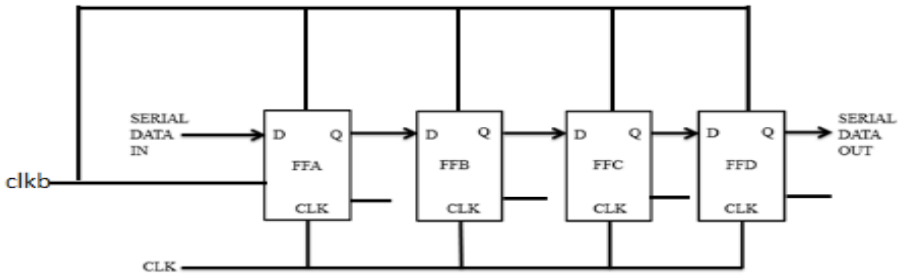

Figure 8:Block Diagram of 4-Bit Shift Registers Using LCNT Based D-Flip Flop

IV RESULTS AND DISCUSSIONS

The designs are implemented using widely used X Manager EDA tools. The simulation and functional verifications are done with the help of Mentor Graphics 130nm technology. The schematic of 4 bit SISO register using conventional D flip flop and its output waveforms are shown in figure 9 and 10.

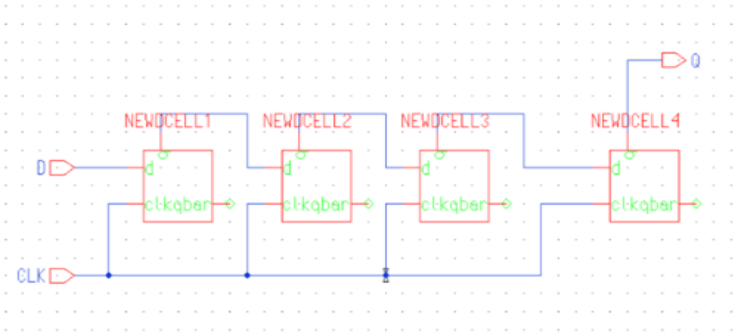

Figure9: Schematic of 4-bit conventional D flip flop

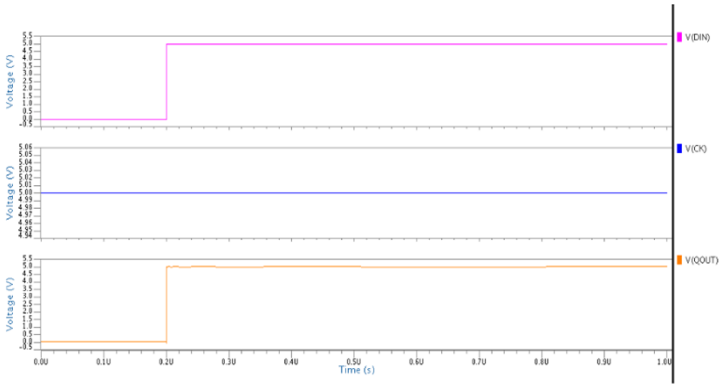

Figure10: Simulation waveforms of 4-bit conventional D-flip flop

The schematic and Simulation waveforms Of 4-Bit SISO using lector based D flip flop is shown in figure 11 and 12.

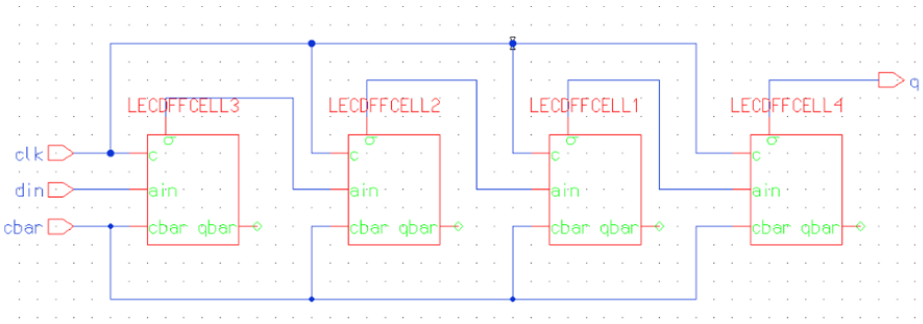

Figure11: Schematic of 4-bit lector based D flip flop

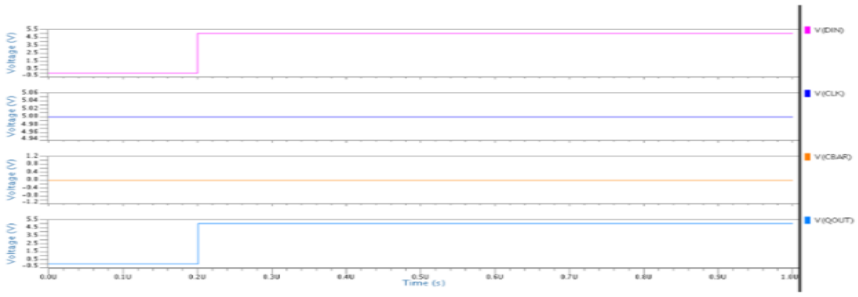

Figure12: Simulation waveforms of 4-bit using lector based D-flip flop

The schematic and Simulation waveforms Of 4-Bit SISO using LCNT is shown in figure 13 and 14

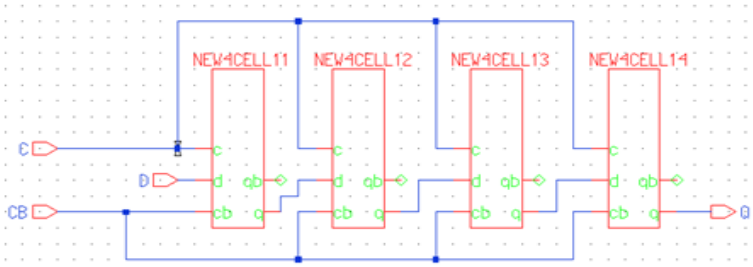

Figure13: Schematic of 4-bit lcnt based D flip flop

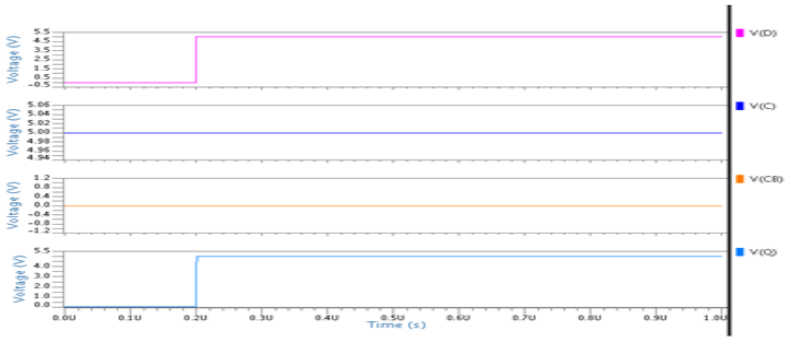

Figure14: Simulation waveforms of 4-bit LCNT based D-flip flop

The comparative analysis of 4-bit SISO register using conventional, lector andLCNT based D flip flops is shown in table1 in terms of power and delay.

Techniques	Power Dissipation	Delay
Conventional D flip flop	21.4906nW	379.32ps
Lector based D flip flop	14.4500nW	854.98ps
Lcnt based D flip flop	10.4710nW	736.60ps

Table 1: Comparison of 4-bit SISO using different techniques

V. CONCLUSION

Flip flops are the basic building blocks of shift registers, counters, storage elements etc. While designing all these power dissipation of flip flop is a major performance deciding factor.LCNT (Leakage control NMOS transistors) technique when applying to the flip flop can greatly reduce its effective power dissipation. The paper presents an efficient implementation of 4-bit SISO register using LCNT based D flip flop with the help of mentor graphics 130nm technology. Further the design is compared with the SISO implemented using conventional as well as lector based flip flop.The simulation results as well the comparative analysis proves that LCNT based SISO register will be a proficient solution to the power efficient SISO register designs.

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