DESIGN AND ANALYSIS OF CURRENT MODE PIPELINED ANALOG TO DIGITAL CONVERTER

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ABSTRACT: An analog to digital converter transforms an analog signal into its digital equivalent. The converter must be compact, highly effective, and power-efficient. In light of recent advances in CMOS technology, circuits running at lower supply voltages have become necessary due to scaling and power considerations. This paper suggests designing and analyzing a current mode pipelined ADC that is compatible with digital CMOS technology. The supply voltage has been adjusted in order to reduce power usage and footprint. Modulating the threshold voltage becomes more difficult when the supply voltage is reduced. This article addresses the design and modeling of a 10-bit converter using a current mirror. The converter uses the GPDK 180nm CMOS technology and the CADENCE SPECTRE tool to function at a supply voltage of 1V. The converter architecture consists of a digital-to-analog converter (DAC) that creates residual current using a basic current subtractor and amplifier, low-resolution, high-speed comparators, and a thermometer-weighted current mode. The combined action of the temperature encoder and current subtractor results in an increase in circuit speed.

Keywords— *CMOS, current mirror, cadence, low power, analog to digital converter, pipelining, gpdk 180nm.*

1. INTRODUCTION

A device known as an analog-to-digital converter is utilized for the purpose of converting an analog voltage signal into a digital numerical representation that is physically comparable to the analog signal. It is the case that the great majority of signals in the physical universe are analog. On the other hand, in order for signals to be processed and utilized in other applications, they need to be digital. An analog-to-digital converter, often known as an ADC, is necessary for data conversion in situations like these. Mixed-signal very large scale integrated circuits (VLSI) systems rely heavily on the analog-to-digital converter (ADC). Commonly, an analog-to-digital converter (ADC) is utilized in conjunction with a pipeline in low-power applications. There are three fundamental properties that define an analog-to-digital converter, also known as an ADC: resolution, speed, and power consumption. Following the completion of the design process for an ADC, it is not possible to alter its characteristics. Despite the fact that it is possible to employ 6-bit precision with an 8-bit ADC,

doing so necessitates entire 8-bit internal processing, which results in a decrease in performance and an increase in power consumption.

An innovative design for a flash analog-to-digital converter (ADC) that possesses the distinctive characteristics of variable resolution and adjustable power is presented in this presentation. Despite the compromise in resolution, it is possible to improve performance while simultaneously reducing the amount of power that is consumed. These characteristics are highly useful in a wide variety of applications that fall under the category of mobile and wireless. It would be nice if the resolution of the ADC could be increased such that it could detect weak signals while simultaneously reducing so that it could detect strong signals. When the resolution is decreased, electricity is saved, which in turn enhances the life of the battery.

Because of the increasing demand for wireless mobile applications, data converters that have resolutions that can be adjusted, signal-to-noise ratios that are satisfactory, and high transfer rates are required. The energy efficiency and cost-effectiveness of these power converters should be taken into consideration. Increasing the efficiency of data converters is necessary in order to meet the requirements of new technologies. In mixed signal architecture, one of the most challenging tasks is the design of data converters that have flexible resolution, high speed, and low power and space consumption.

2. REVIEW OF LITERATURE

Within the context of a pipelined 13-bit ADC, the work conducted by M. A. and Sani Anasi Hamoui provides a description of the implementation of digital background calibration. In addition to that, they utilized SIMULINK in order to test the behavioral elements of this technology. During the investigation, it was considered that there was a mismatch between the capacitors (σ = 0.25%). Upon analysis, it was discovered that the signal-to-noise ratio (SNR) had increased from 10 bits to 12.5 bits, and the spurious-free dynamic range (SFDR) had reached 95 decibels.

The Signal-to-Noise and Distortion Ratio (SNDR) of 46.9 dB and the Spurious-Free Dynamic Range (SFDR) of 48.9 dB in an 11-bit pipelined Analog-to-Digital Converter (ADC) were both increased to 70 dB and 60 dB, respectively, by the implementation of an approach that was given by Imran Ahmed in the year 2008. Due to the utilization of a fabrication prototype that utilized a 0.18 µm process for the purpose of calibrating the ADC, this increase was successful. For the purpose of completing the calibration procedure, the backend utilized a clock cycle of 104. In 2009, the authors started applying the split calibration approach on a 12-bit ADC in order to accomplish the goal of improving the SFDR and SNDR capabilities of SIMULINK. This article covers gain error in relation to capacitor mismatch in the context of the topic. The results of the behavioral simulation showed that the SNDR and SFDR values had significantly improved, going from 56.4 to 73.8 dB. This indicates that the simulation was successful. There were roughly 105 cycles that were necessary for the calibration operation.

Harmonic distortion correction (HDC) and DAC noise cancellation (DNC) are two background

calibration methods that were established by the authors, A. Both Panigada and I. Galton, in order to address concerns of capacitor mismatch and gain inaccuracy in pipelined ADCs. For the purpose of correcting gain error, the HDC method was utilized, which resulted in an SNDR of 70 dB and an SFDR of 85 dB. [6] This was achieved with the utilization of a 90nm CMOS technology that required 130mW of more power. 2011 saw the beginning of an endeavor that was spearheaded by Lee and Flynn, which involved the utilization of a Successive Approximation Register Analog-to-Digital Converter (SAR ADC). This analog-to-digital converter (ADC) demonstrated exceptional energy efficiency, prompt operation, and good resolution while consuming a small amount of power. This remarkable result was accomplished by employing a method that did not call for any calibration to be performed. CMOS production techniques at 65 and 90 nm at Nyquist resulted in a throughput of 50 MS/s and an effective bit count of 10.4 b. This was achieved on the Nyquist facility.

In order to achieve the dual objectives of low error gain and power consumption, the author designed a pipelined 10-bit Analog-to-Digital Converter (ADC) that makes use of digital calibration techniques and toggling operational amplifiers. This CMOS technology, which has a pitch of 65 nanometers, is designed to be utilized in the ADC. Based on the findings of the inquiry, the SNDR and SFDR values were found to be 55.4 dB and 67.2 dB, respectively. All of the aforementioned outcomes were accomplished using a power supply of 1V, a chip area of 0.36 mm2, and a relatively low power consumption of 26.6 mW. A time-interleaved SAR ADC prototype that was constructed using 65 nm CMOS technology was disclosed in a publication that was published in 2014. The purpose of this work is to offer a method that employs a Flash ADC as a baseline for a timing skew calibration strategy. This ADC demonstrated a significantly faster rate of operation when compared to eight other SAR ADCs.

Digitally calibrating circuit faults was accomplished by the authors in 2015 through the utilization of a totally deterministic technique. Additionally, a 12-bit split-stage multistage pipeline ADC was utilized for this technique. A CMOS with a frequency of 200 MS/s and a 40 nm was calibrated in order to solve concerns regarding capacitor mismatch and amplifier gain volatility. This article demonstrates how to make use of behavioral modeling in order to determine the dimensions and power consumption of a 40nm 12-bit pipelined automated digital converter (ADC). According to the findings, the ADC consumes 54 milliwatts of electricity and occupies 0.42 millimeters squared in area.

The authors, A. Fahmy and colleagues, emphasized the programmability and reconfigurability of the stochastic advanced digital converter (ADC). In order to accomplish this, the entire design was divided into eight channels, each of which had its own control word that was ten bits long. Verilog and digital design tools were utilized in order to acquire the outcomes of the synthesis that was performed using a 130nm CMOS technology. A supply voltage of 0.7V was used to assess the spurious-free dynamic range (SFDR) as well as the signal-to-noise and

distortion ratio (SNDR). A separate study demonstrated and detailed how the LMS algorithm, which stands for least mean squares, can be utilized for background calibration in pipelined ADCs to remove conversion errors and apply the DRDE method, which stands for digitized residue distance estimation. An strategy to calibrating digital backdrops is proposed by the authors (M.A. Whencemorelhood et al.), which makes use of the LMS algorithm to account error gains and capacitor mismatch. The amount of time required for conversion is much less than that required by other LMS techniques that are comparable and documented in a study written by B. 2014 saw the occurrence of Zenali. A 12-bit 100MS/s split pipelined ADC was utilized for the purpose of simulation by the researchers.

In 2005, the authors, L. F. Dorrer and himself, elaborated on the fact that with a tracking ADC, it is possible to achieve low power consumption by utilizing three different comparators. There is a correlation between the enhanced and optimized stability of the loop and the reduction in the amount of time that the loop delays. After doing empirical study, it has been determined that the analog-to-digital converter (ADC) needs a power supply voltage of 1.5 volts and a clock frequency of 104 megahertz in order to perform properly.

An additional contribution made by A. was the development of a time-interleaved analog to digital converter (TI-ADC) that possessed the highest sampling rate and bandwidth. Notable authors include Zandieh and others. In order to successfully accomplish this, track and hold amplifiers, a low-power comparator, and a trigger are utilized in order to obtain a resolution of 5 bits. Using a digital backdrop calibration approach is something that the author suggests doing in order to improve the functionality of the 12-bit pipelined ADC and address issues that are typical in 90nm CMOS technology. These concerns include capacitor mismatch, gain errors, and nonlinearities.

Comparative research on a wide variety of low-power CMOS architectures was carried out by KB Vaibhav and colleagues while they were conducting a review of high-speed analog-to-digital converters (ADCs). This piece of writing provides in-depth explanations of a number of different types of analog-to-digital converters (ADCs), including Flash ADCs, pipelined ADCs, SAR ADCs, subranging and two-step ADCs, interpolating ADCs, and folding ADCs. The fact that these ADCs are able to function at high speeds while simultaneously conserving power makes them an excellent choice for hybrid ADC systems. This effort also focuses on the development of a hybrid analog-to-digital converter (ADC) for use in applications that call for a sampling rate of one gigahertz per second and a resolution of six bits.

A dual split 3-section capacitive array DAC (Digital-to-Analog Converter) with a SARADC (Successive Approximation Register Analog-to-Digital Converter) was presented by Savitha and colleagues in 2019. This DAC was designed specifically for Internet of Things (IoT) applications. In order to obtain great accuracy in peer communication at CMOS (Complementary Metal-Oxide-Semiconductor) development costs equivalent to those of a 14-bit SAR ADC, the objective of this design was to achieve this goal.

For the purpose of enhancing gain and integral nonlinearity (INL) errors, T. Hung and colleagues developed a split ADC that included digital background calibration and was implemented in a 12-bit 400MS/s pipelined ADC. To reduce the amount of power consumed by the other 12-bit amplifiers, the ADC made use of Class C in a number of different rate-enhancing ways. As stated by Mohd Naved and colleagues, the effectiveness of the slew rate is greatly enhanced by the implementation of this method. Due to the fast speed of the device, researchers investigate and describe the usage of Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) in a variety of domains. These fields include biomedical applications, wireless sensors, and receivers. There are several applications for the flash ADC, which is an alternative type of analog-to-digital converter. Some of these applications include radar, wireless sensor networks, high-speed instrumentation, and digital storage oscilloscopes.

3. BACKGROUND WORK

The goal is to study, develop, and build a 10-bit current mode pipelined analog-to-digital converter. The current mirror circuit is the focal focus of the design process. The thermometer's current comparator and encoder are then devised. The intended components are then blended to get correct results.

Current Mirror

Current mirrors are an essential component of current mode circuits and serve vital purposes. In very large scale integration (VLSI) technology, transistors with the tiniest feature sizes are used extensively. In general, it is preferable to have a circuit that has a high output resistance and uses a small amount of channel length modulation. There is a wide selection of contemporary mirrors available. The output resistance of conventional current mirror-based analog circuits must be increased in order to function properly. The electrical current that is flowing via M1 is connected to the VGS1 wire. Due to the fact that VGS1 and VGS2 are identical, the current that flows through M2 does not change even when it is already saturated. The utilization of the regulated gate current mirror that is presented in this study has the potential to enhance this technology, despite the fact that its output impedance is extremely low.

One does not need to make use of compensating or biassing hardware in order to raise the output impedance of a regulated gate current mirror. The implementation of cascaded current mirrors is accomplished through the utilization of NMOS and PMOS transistors, specifically M1 through M4. The output impedance of the NMOS circuit is increased as a result of the components M7 and M8. The aspect ratio of Mn5 and Mn7 is identical, which can be determined by first equating VGS5 to VGS7 and then equating VDS6 to VDS8. There is no difference between the two. As a result, the values of VGS6 and VGS8 are comparable. VGS6 is equivalent to VGS2, VDS2, and VDS4, and as a result, VDS2 is equal to VDS4, and Iin is equal to Iout.

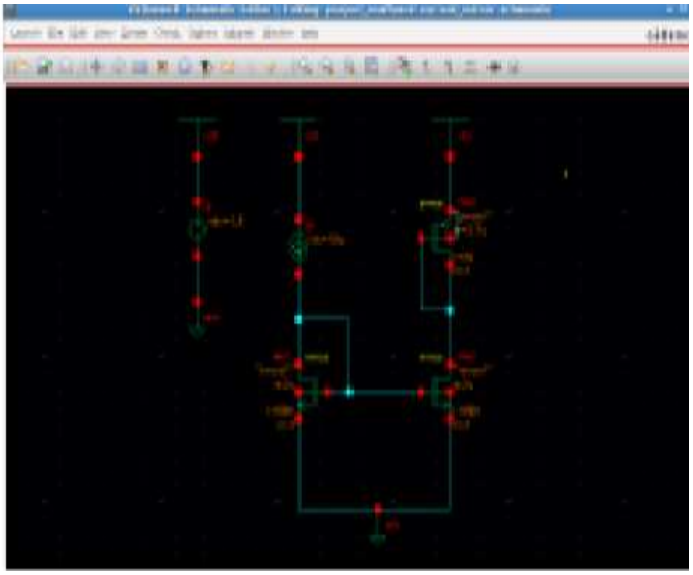

Fig.1: An illustration of the basic layout of components in a modern mirror.

Comparators

The ADC's architecture is fundamentally based on compatibility. This component compares an input voltage (Vin) to a reference voltage (Vref) and converts the difference into a binary signal, "1" or "0". If the voltage Vin exceeds the reference voltage Vref, the comparator outputs the logic level "1". Alternatively, the value "0" will be shown. This design uses two N-1 differential amplifiers as comparators for the flash-ADC.

A logic "1" is produced when the input signal voltage exceeds the reference voltage, and a logic "0" is produced when the input signal voltage falls below the reference level. The comparators produce 2N-1 output levels that are regulated by the reference voltage.

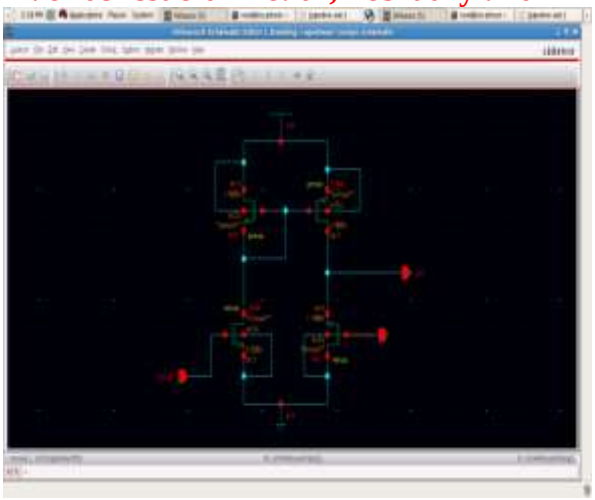

Fig 2: A schematic demonstrating the individual components and assembly of a comparator.

Current Amplifier and Subtractor

Before moving on to the next phase, the current provided to the current subtractor and amplifier must be amplified and then subtracted. The nMOS circuit has a one-to-one connection with the input current, but the pMOS circuit amplifies the reference circuit. Furthermore, the MSW transistor works as a switch. This switch is enabled when the value of Iref needs to be subtracted from Iin. When the switch is turned off, the PMO module increases the subtracted current to match the input current.

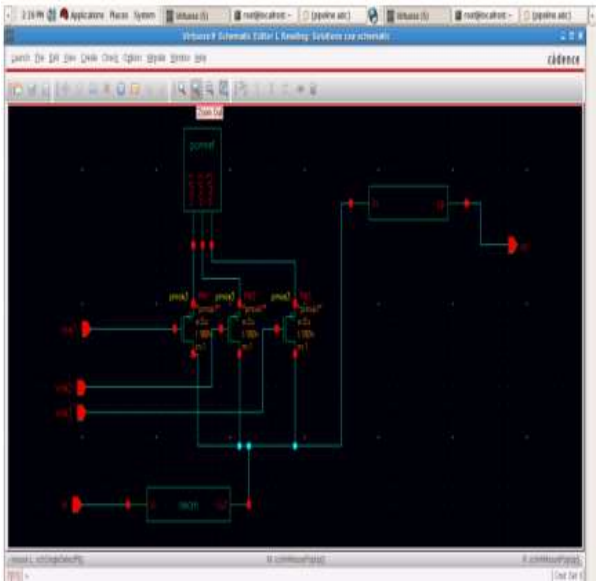

Fig 3: The picture depicts the components and structure of community-supported agriculture (CSA).

Thermometer Encoder

The output of the three comparators is effectively converted into a two-bit encoded format using a thermometer encoder. The diagram below depicts the modern mirror's VLSI schematic architecture.

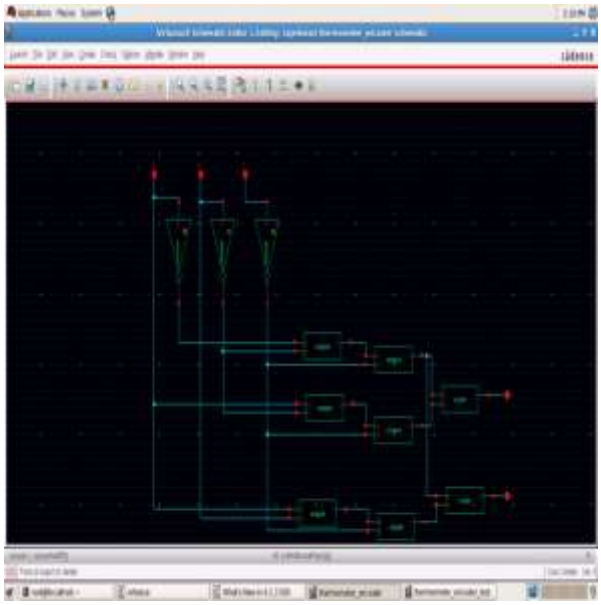

Fig 4: A schematic demonstrating the construction of a thermometer encoder.

Current Mirred Pipelined ADC

The best strategy is to use a current as the input and then analyze it in respect to other currents. Nonetheless, the ADC's output bits retain their logic values. The primary difficulty with the architecture is its high electricity consumption. Every Analog-to-Digital Converter (ADC) includes a temperature encoder, a three-level comparator, and a flash ADC with two bits. To improve realism, the reference current is increased from 0µA to 10µA. To improve efficiency and prevent the amplifier from increasing a current of 0µA, the same current will be removed before transmission. The diagram shows the schematic of a modern mirror-pipelined ADC.

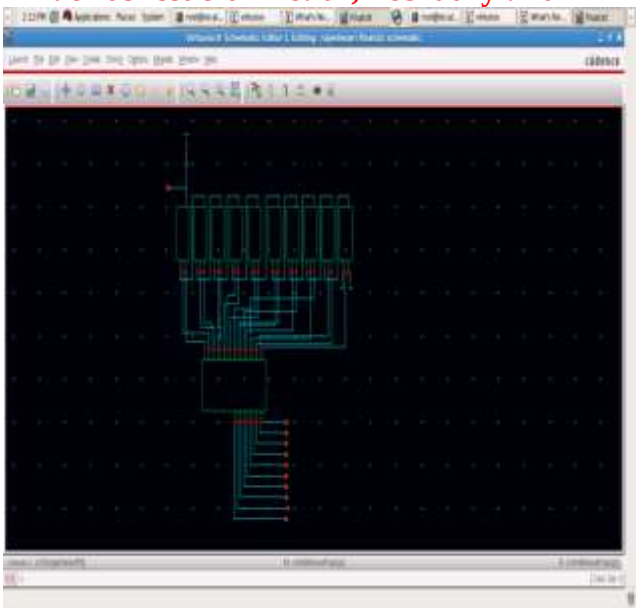

Fig 5 The ADC is now functioning in pipelined mode.

4. EXPERIMENTAL OUTCOMES

The recommended Analog-to-Digital Converter (ADC) is created and executed in IC version 6.1, using the popular gpdk180nm technology and the Cadence Virtuoso tool. The subsequent findings were obtained.

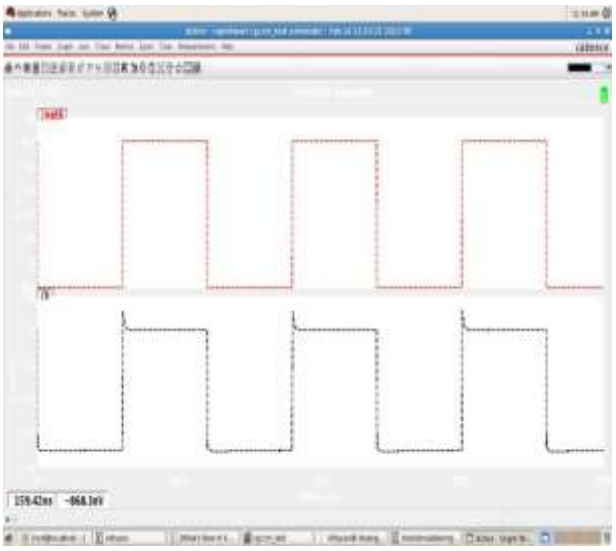

Fig 6: The basic current reflects the geometry of the output waveform.

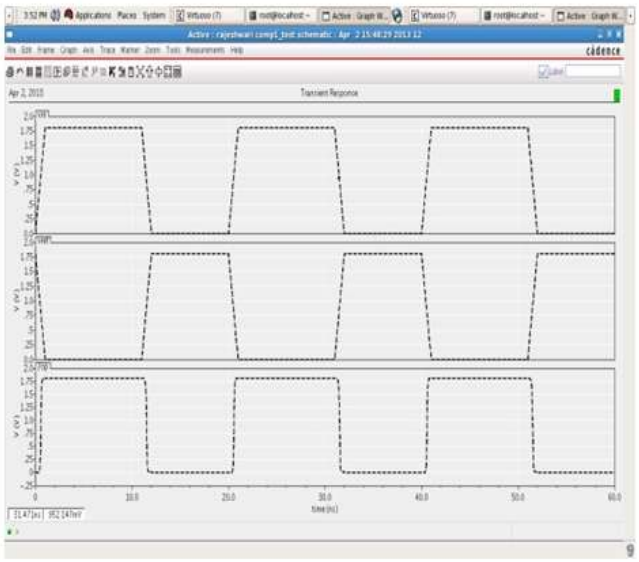

Fig 7: The waveform generated by the comparator.

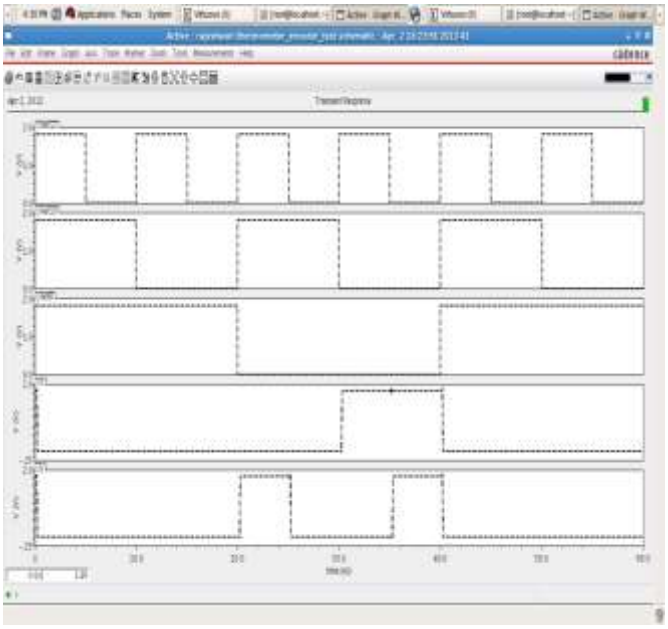

Fig 8: The waveform generated by the thermometer encoder.

5. CONCLUSION

As shown in the schematic picture of the design, the following components are included: a primary current mirror, a comparator stage, a current subtractor cum amplifier stage, a temperature encoder stage, and a digital error correcting stage. With a resolution of 10 bits, the current pipelined ADC requires a supply voltage of 4V and can accept analog input voltages ranging from 0 to 1.8V. Additionally, it has a supply voltage requirement of 4V. Ten bits is the resolution that the ADC can achieve. An analog-to-digital converter (ADC) in version IC 6.1 of the standard gpdk180nm technology is designed and implemented with the help of the Cadence Virtuoso tool.

FUTURE WORK

One of the goals that can be accomplished is to enhance the performance of the design that is presented in this paper. With the resolution increased to 15 bits, there is the possibility that the precision will be improved. Through the use of the Cadence software, digital laboratories are able to generate Verilog code, which can then be executed on hardware. Through the utilization of a wide range of low power comparators and encoding techniques, it is possible to decrease the amount of power that is consumed by a current mode pipelined ADC.

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