A FPGA ARCHITECTURE OF ADDRESS GENERATOR FOR WIMAX DEINTERLEAVER

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Abstract— In this project, a low-intricacy and innovative technique is proposed to efficientlyimplementtheaddressgenerationcircuitryofthe2-DdeinterleaverusedintheWiMAX transreceiver using the Xilinx field-programmable gate array (FPGA). Thefloorfunctionassociatedwiththeimplementationofthesteps,requiredforthepermutation of the incoming bit stream in channel Interleaver/deinterleaver for IEEE802.16e standard is very difficult to implement in FPGA. A simple algorithm alongwith its mathematical background developed in this brief, eliminates the requirementof floor function and thereby allows low-complexity FPGA implementation. The useof an internal multiplier of FPGA and the sharing of resources for quadrature phase-shift keying, 16-quadrature-amplitude modulation (QAM), and 64-QAM modulationsalong with all possible code rates makes our approach to be novel and highly efficientwhencomparedwithconventionallook-uptable-basedapproach.Theproposedapproach exhibits significant improvement in the use of FPGAresources.Exhaustivesimulationhasbeen carriedouttoclaimsupremacyofourproposedwork.TheIEEE802.16standard,commonlyknownas WiMAX,isthelatesttechnology that has promised to offer broadband wireless access over long distance. Since 2001 WiMAX has evolved from 802.16 to 802.16d for fixed wireless access,andtothenewIEEE802.16estandardwith mobilitysupport.

INTRODUCTION

WiMAX is based on the IEEE 802.16 standard for BWA system. IEEE 802.16d, now known as, IEEE802.16-2004 defines fixed BWA (FBWA) in the frequency band of 2 to 11GHz [2]. Amended IEEE802.16e adds mobility support to IEEE 802.16 and defines standard for mobile BWA (MBWA) in thefrequencyband 2to6GHz.TypicaldatarateinIEEE802.16eis5

Mbpswithbandwidth1.25 to 20 MHz.BothIEEE802.16-2004andIEEE802.16e permitNonLine ofSight(NLOS)connectivity[3]. OrthogonalFrequencyDivisionMultiplexing(OFDM) [3]techniqueofferspromisingsolutionthathasgainedtremendousresearchinterestinrecentyears duetoitshightransmissioncapabilityandalsofor

alleviating the adverse effects of Inter Symbol Interference (ISI) and Inter Channel Interference (ICI). Inan OFDM system, the data is divided into multiple parallel substreams at a reduced rate, and each ismodulated and transmitted on a separate orthogonal subcarrier. This increases symbol duration andimproves system robustness [4]. OFDM is achieved by providing multiplexing on users' data streams onboth uplink and downlink transmissions. OFDM is the fundamental building block of the IEEE 802.16standard.

Interleaving plays a vital role in improving the performance of Forward Error Correction (FEC)codes in terms of Bit Error Rate (BER). Interleaving is the process to rearrange code symbols so as tospread burst of errors into random like errors and thereafter FEC techniques could be applied to correctthem. Inconventionalblockinterleaver[5],thebitsreceivedfromtheencoderarestoredrowwiseintheinterleaver's memory and read column wise. WiMAX uses a special type of block interleaver in whichthe InterleaverDepth(ID)andpatternvarydependingonthe code rate andmodulationtype.

BROADBAND wireless access (BWA) is continuously becoming a more challenging competitorto the conventional wired last mile access technologies [1]. IEEE has developed standards for mobileBWA (IEEE 802.16e) popularly referred to as mobile WiMAX [2]. The channel interleaver employed inthe WiMAX transreceiver plays a vital role in minimizingthe effect of burst error. In this brief, a novel,low-complexity, high-speed, and resource-efficient address generator for the channel deinterleaver usedin the WiMAX transreceiver eliminating the requirement of floor function is proposed. Very few worksrelated to hardware implementation of the interleaver/deinterleaver used in a WiMAX system is availablein the literature. The work in [3] demonstrates the grouping of incoming data streams into the block toreduce the frequency of memory access in a deinterleaver using a conventional look-up table (LUT)-based CMOS address generator for WiMAX. Khater *et al.* [4] has described a hardware descriptionlanguage (VHDL)- based implementation of address generator for IEEE 802.16e channel interleaver withonly a 1/2 code rate. In [5], the authors have described a finite-state machine (FSM)-based addressgenerator of the same interleaver for all permissible code rates and modulation

schemes. Both [4] and [5]aretestedonthefield-programmable gatearray(FPGA)platform.

PROPOSED TECHNIQUE

Out of all the 2D realization of WiMAX channel interleaver for efficient hardware implementation and Novel design of address generator for WiMAX multimode interleaver using FPGAbased finite state machine, 2D realization of WiMAX channel interleaver for efficient hardware implementation has mathematical limitations. Whereas Novel design of address generator for WiMAXmultimode interleaver using FPGA based finite state machine incorporate random code rates with hardware efficient. In upcoming section we have results and discussion with final conclusion on this project.

In this project, a novel, low-complexity, high-speed, and resource-efficient address generator forthechanneldeinterleaverusedintheWiMAXtransreceivereliminatingtherequirementoffloorfunctionis proposed. As compared with the complicated and lengthy expressions, particularly for 16-QAM and64-QAM, due to the 2-D translation, a compact and user-friendly mathematical representation andsubsequentalgorithmis proposed.

LITERATURE REVIEW

1.AddressGeneratorforHighPerformanceWiMAXDeinterleaver:

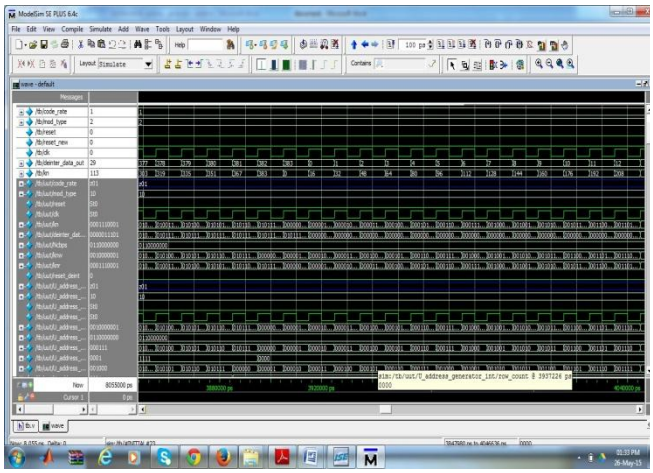
The main aim of this project is to generate the address generation circuitry of Deinterleaver usedin the WiMAX transreceiver using the Xilinx Field Programmable Gate Array (FPGA). The floorfunction associated with the implementation of FPGA is very difficult in IEEE 802.16e standard. So weeliminate the requirement of floor function by using a simple mathematical algorithm. Some modulationslike QPSK, 16-QAM and 64-QAM along with its code rates make our approach to be novel and highefficient.

2.AnImprovedLUTBasedReconfigurableMultimodeInterleaverforWLANApplication:

IEEE802.11basedwirelessLANisconsideredtobe themostprevailingbroadbandindoornetworking technology. Fast spread of wireless data communication systems and the ever increasingdemand for faster data rates require quick design, implementation and test of new wireless algorithms fordatacommunications.Inthispaperwepresentanimprovedtechniquetomodelthemultimodeinterleaverused in IEEE 802.11a and IEEE 802.11g based WLAN in VHDL using Xilinx ISE.

SIMULATIONRESULTS

FORQPSK,CODERATE=0,Ncpbs=64



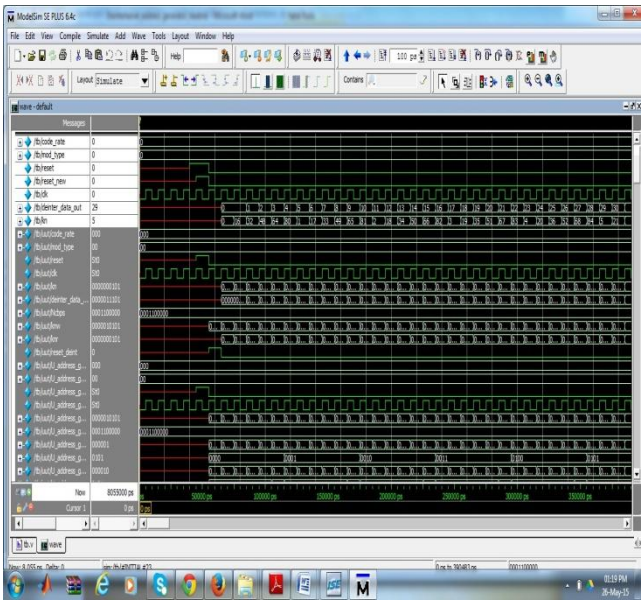
FORQPSK,CODERATE=234,Ncpbs=384

CONCLUSION

In this paper, proposed a novel algorithm along with its mathematical formulation, includingproof for address generation circuitry of the WiMAX channel deinterleaver and interleaver supporting allpossible code rates and modulation patterns as per IEEE 802.16e. The proposed algorithm is convertedinto an optimized digital hardware circuit. The hardware is implemented on the Xilinx ISE 12.3 usingVerilog. Comparison four proposedworkwithaconventionalLUTbasedmethodandalsowitharecentworkshowsignificantimprovementonresource utilizationandoperatingfrequency.

FUTURESCOPE

Infuture,wecanimplementtheWiMaxtransceiverwithhighermodulationtechniques.TheLUTswillbe modified and modeled using FPGA's



embedded memory, i.e., blocks RAM, to further reduce thememoryaccess time.

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