

FAST BINARY COUNTERS AND COMPRESSORS GENERATED WITH BITONIC SORTING NETWORKS

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Abstract —In this article, we present a novel method of fast saturated binary counters and exact/approximate (4:2) compressors based on the sorting network. The inputs of the counter are asymmetrically divided into two groups and fed into sorting networks to generate reordered sequences, which can be solely represented by one-hot code sequences. Between the reordered sequence and the one-hot code sequence, three special Boolean equations are established, which can significantly simplify the output Boolean expressions of the counter. Further, this project is enhanced by using parallel sorting algorithms for finding/ sorting M largest values from N inputs and then design scalable architectures based on proposed algorithms. For finding the largest values the iterative sorting techniques also proposed. BITONIC SORTING is one type of efficient such algorithm for implementing with optimised parameters.

INTRODUCTION

Energy minimization is full-size stipulations in really any digital fabric, specifically the available bones like PDAs, tablets, and colourful bias. It's astonishingly desired to attain this minimization

with negligible prosecution (pace) discipline (1). Motorized sign coping with (DSP) blocks are usually demanded in transportable hall for admitting unique media operations. The computational middle of those locations is the ALU in which the accruals and will increase are the full-size component (6). The accruals performs first exertion withinside the strolling elements that may activates most operation of electricity and energy. A full-size variety of the DSP facilities perform photograph and videotape coping with computations in which final effects are furthermore filmland or recordings equipped for mortal applications. It works with to head for approximations for running on the rate and electricity withinside the variety- scraping circuits. This starts from the restricted perceptual capacities in noticing a photograph or a videotape for individualities. Notwithstanding the photograph and videotape strolling operations, there are unique areas in which the perfection of the calculation obligations isn't always introductory to the software of the frame (see (2), (3)). Rough figuring offers an fineness, pace and energy/ electricity application. The

advantage of meant multiplier lessens the boob price and advantage fast. For amending the department mistake think approximately exertion and a reminiscence flip overhead is demanded for the each operand is wanted which builds the time detention for entire duplication process (4). At unique diploma of mirrored image consisting of circuit, rationalization and layout conditions the estimate is handled (5). In the bracket for estimate techniques in paintings, colourful coming near calculation shape blocks, like adders and multipliers, at colourful plan conditions had been endorsed in unique designs (6), (7). Broken parade multiplier became meant for whole VLSI perpetration (8).

the distance of the proposed configuration will now no longer proliferation with the network.

IMPLEMENTATION:

To begin with, as displayed in below Fig. because of the manner that "1" is lesser than "0", all the "1"s are on the loftiest factor of the association if there stay "1"s, and all the "0"s are on the decrease a part of the race if there stay "0"s. In the occasion that there stay each "1"s and "0"s, there ought to be a scenario withinside the reordered race in which there may be the crossroad of "1" and "0". If there are because it were "1"s or "0"s, we will cope with the grouping with the aid of using softening constant the fewest bit "1" on the pinnacle and the fewest bit "0" on the decrease a part of the reordered association to insure that- crossroad continuously exists. Second, the reordered association has a analogous all out range of "1"s and "0"s because the first grouping (the benefactions of arranging associations). Albeit the gentled "1" might effect the all out range of "1"s withinside the gentled association, it is constant, so we forget about it at the same time as counting.

EXISTING TECHNIQUE

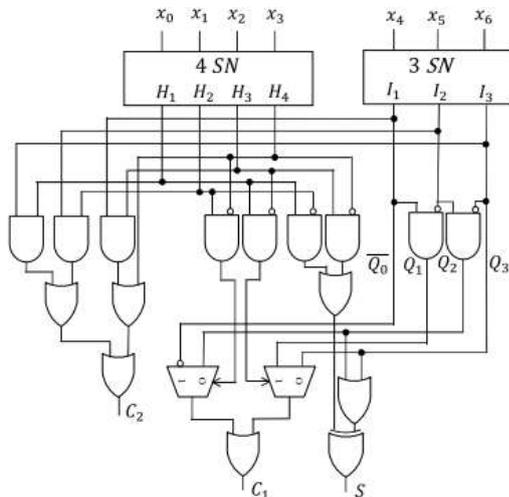


Fig: Overall (7,3) counter circuit

The whole engineering is displayed in above Fig. Easily the methods from members of the family H and I to C2, C1, and S are certainly independent. Builds the network of the circuit. Notwithstanding, as might be mentioned latterly,

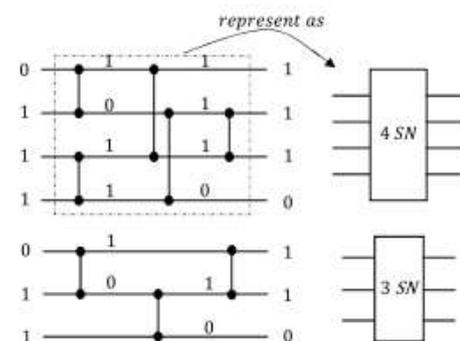


Fig. Three- and four-way sorting networks.

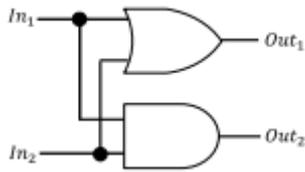


Fig. Two-input binary sorter

We provide an phrase version association (0, 1, 1, 1) addresses the donation of 4- manner arranging affiliation (four SN), and race (0, 1, 1) addresses the donation of 3- manner arranging affiliation (three SN). For each four SN and three SN, the phrase groupings are reordered as the larger range on the pinnacle and the extra modest range at the bottom after 3 layers of genre.

PROPOSED METHOD

Bitonic kind is one of the quickest arranging associations. An arranging networks an exceptional kind of arranging computation, where the arrangement of correlations is not information inferior. This makes arranging networks applicable for prosecution in outfit or inparallel processorarrays. The arranging network bitonic sort comprises of $\Theta(n \cdot \log(n) \cdot 2)$ comparators. It has a analogous asymptotic intricacy as odd-even mergesortand shellsort. Albeit an arranging network with just $O(n \cdot \log(n))$ comparators is known (AKS 83), because of its huge harmonious it's further slow than bitonic kind for all realistic issue sizes.

In the accompanying, bitonic kind is created grounded on the 0-1-standard. The 0-1-standard expresses that a comparator network that sorts each arrangement of 0's and 1's is an arranging association, for illustration it sorts each

arrangement of tone-assertive rates. Bitonic mergesort is an equal computation for arranging. It's likewise employed as a development fashion for erecting an arranging association. The computation was conceived by Ken Batcher. The posterior arranging networks comprise of comparators and have a postponement of, where is the volume of effects to be arranged.

An arranged grouping is a monotonicallynon-diminishing (ornon-expanding) race. A bitonic grouping is an arrangement with for a many, or a round shift of such a race

The 16 figures enter at the benefactions at the left end, slide along every one of the 16 position cables, and exit at the results at the right end. The association is intended to sort the factors, with the biggest number at the base.

The bolts are comparators. At whatever point two figures arrive at the two homestretches of a bolt, they're varied with guarantee that the bolt highlights the bigger number. In case they're meddled up, they're traded. The hued boxes are only for representation and have no impact on the computation.

Each red box has a analogous construction each donation to the top half is varied with the comparing input in the base half, with all bolts pointing down (dull red) or all up (light red). In case the sources of word end up shaping a bitonic grouping, also, at that point, the result will frame two bitonic relations. The top portion

of the result will be bitonic, and the base half will be bitonic, with each element of the top half not exactly or original to each element of the base half (for dull red) or the other way around (for light red). This thesis is not tone-apparent, still can be verified via cautiously considering every one of the cases of how the different information sources may look at, exercising the zero-one standard.

The red boxes consolidate to frame blue and green boxes. Each similar box has a analogous design a red box is applied to the whole word arrangement, also, at that point, to every 50 of the outgrowth, also, at that point, to every 50 of every one of those issues, etc. All bolts point down (blue) or all point up (green). This construction is known as a butterfly association. In case the donation to this case turns out to be bitonic, also, at that point, the result will be completely arranged in expanding request (blue) or dwindling request (green). Assuming a number enters the blue or green box, the main red box will sort it into the right 50 of the rundown. It'll also, at that point, go through a more modest red box that sorts it into the right quarter of the rundown inside that half. This proceeds until it's arranged into precisely the right position. In this way, the result of the green or blue box will be completely arranged.

The green and blue boxes consolidate to frame the whole arranging association. For any private grouping of sources of word, it'll sort them

directly, with the biggest at the base. The result of each green or blue box will be an arranged grouping, so the result of each brace of touching records will be bitonic, on the grounds that the stylish one is blue and the last bone is green. Every section of blue and green boxes takes N arranged relations and links them two by two to shape $N/2$ bitonic groupings, which are also arranged by the cases in that member to frame $N/2$ arranged groupings. This cycle begins with each word viewed as an arranged rundown of one element, and proceeds through every one of the sections until the last connections them into a solitary, arranged rundown. Since the last stage was blue, this last rundown will have the biggest element at the base.

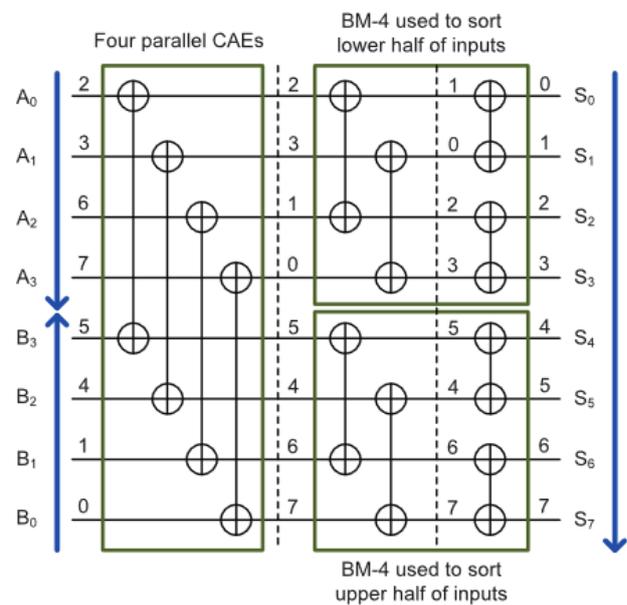
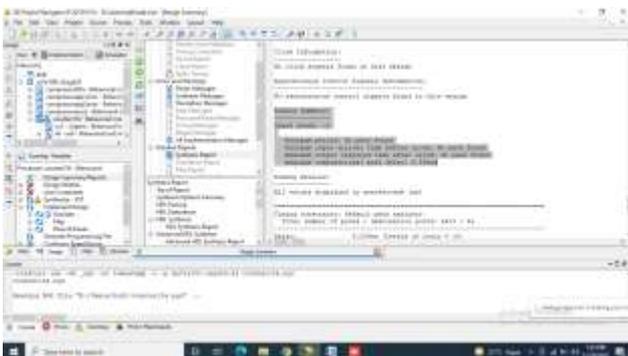
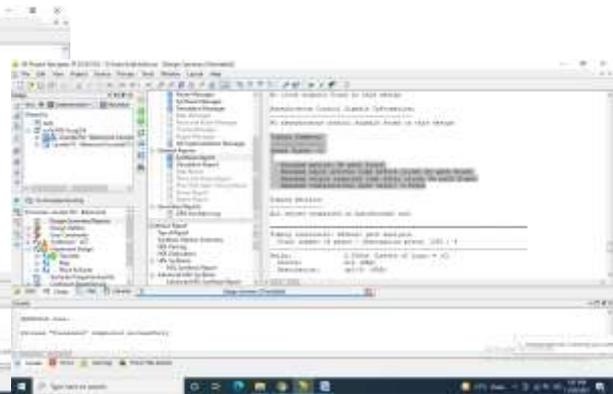
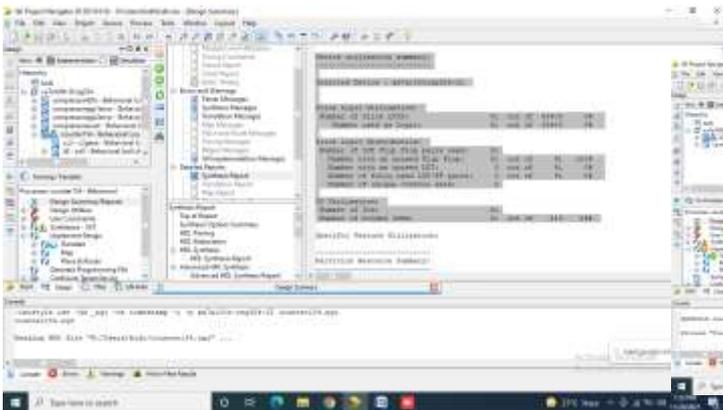
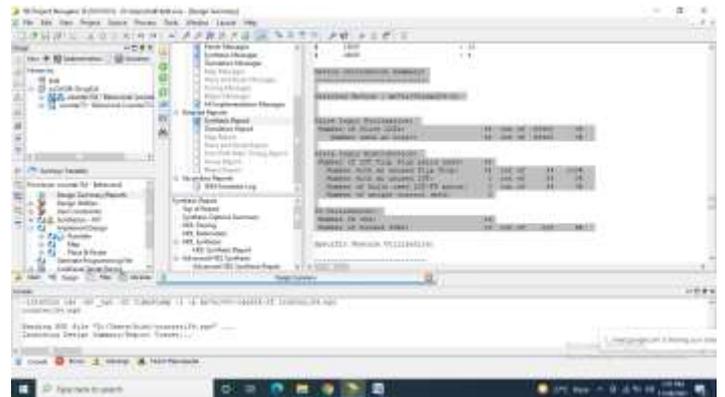
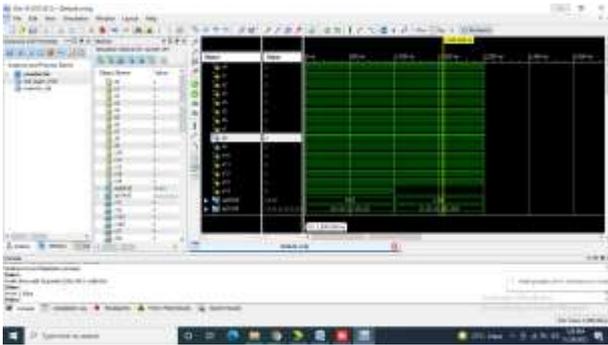


Fig. An increasing 8-input bitonic merging unit

SAMPLE RESULTS

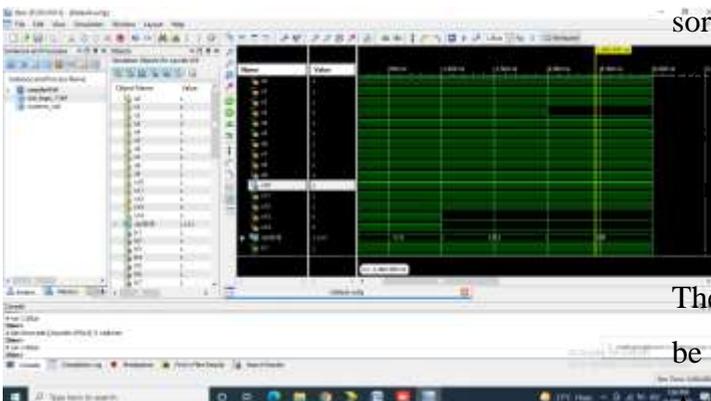
EXISTING RESULTS:



CONCLUSION

In this paper, a plan strategy for region viable and speed effective counter is planned and reproduced. A twofold counter in view of a novel symmetric piece Aggregate and convey computation approach is proposed. In this process, a new counter design method based on a sorting network is proposed, and we construct (7,3), (15,4) counters based on this biotonic sorting method. Proposed counters are more flexible than existing designs because it achieves less delay when the speed is critical and performs in better in ADP

PROPOSED RESULTS:



FUTURE SCOPE:

The image, videos and the clarity of videos can be checked by using approximate multipliers. And that are tired to match the clarity of the

exact multipliers. For faster multiplication we have use Brent Kung Adder to reduce area and to increase speed we can use Kogge Stone Adder.

REFERENCES

- [1] Wen-Chang Yeh and Chein-Wei Jen, "High-speed Booth encoded parallel multiplier design," IEEE Trans. on Computers, vol. 49, isseu 7, pp. 692-701, July 2000.
- [2] Jung-Yup Kang and Jean-Luc Gaudiot, "A simple high-speed multiplier design," IEEE Trans. on Computers, vol. 55, issue 10, Oct. pp. 1253-1258, 2006.
- [3] Shiann-Rong Kuang, Jiun-Ping Wang and Cang-Yuan Guo, "Modified Booth multipliers with a regular partial product array," IEEE Trans. onCircuit and Systems, vol.56, Issue 5, pp. 404-408, May 2009.
- [4] Li-rong Wang, Shyh-Jye Jou and Chung-Len Lee, "A well-structured modified Booth multiplier design," Proc. of IEEE VLSI-DAT, pp. 85-88, April 2008.
- [5] A. A. Khatibzadeh, K. Raahemifar and M. Ahmadi, "A 1.8V 1.1GHz Novel Digital Multiplier," Proc. of IEEE CCECE, pp. 686-689, May 2005.
- [6] S. Hus, V. Venkatraman, S. Mathew, H. Kaul, M. Anders, S. Dighe, W. Burleson and R. Krishnamurthy, "A 2GHZ 13.6mW 12x9b mutiplier for energy efficient FFT accelerators," Proc. of IEEE ESSCIRC, pp. 199-202, Sept. 2005.