A SURVEY ON AXBMS: APPROXIMATE RADIX-8 BOOTH MULTIPLIERS FOR VLSI IMPLEMENTATION OF BOOTH MULTIPLIER FOR FPGA

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ABSTRACT: This paper proposed low latency VLSI implementation of booth multiplier for FPGA- applications. Simulation is done using Xilinx ISE software. Simulation results shows that the performance improvement in terms of speed and latency. The multiplication operation is present in many parts of a digital system or digital computer, most notably in signal processing, graphics and scientific computation. With advances in technology, various techniques have been proposed to design multipliers, which offer high speed, low power consumption and lesser area. Thus making them suitable for various high speeds, low power compact VLSI implementations. These three parameters i.e. power, area and speed are always traded off. Now days Analog systems are replacing by digital systems because of its high speed performance, takes less area and less power dissipation. Multiplication is one of the most important and basic arithmetic operation that constitute programs.

INTRODUCTION

Digital multiplier is one of the key operations of the ALU of processor. The Xilinx seven series logic FPGA VLSI processor are using under 5G constraints. Research are continue going on various existing multipliers for enhancing in terms of performance improvement like high speed, low delay, low area, low power etc. In addition to the image and video processing applications, there are other areas where the exactness of the arithmetic operations is not critical to the functionality

of the system (see [2],[3]). Approximate computing provides an accuracy, speed and power/energy consumption. The advantage of approximate multiplier reduces the error rate and gain high-speed. For correcting the division error compare operation and a memory look up is requiredfortheeachoperandisrequiredwhich increasesthetimedelayforentiremultiplicati onprocess[4].Atvariouslevelofabstractionin cludingcircuit,logicandarchitecturelevelsth eapproximationis processed [5].

In the category for approximation methods in function, a number of approximatingarithmetic building blocks, such as adders and multipliers, at different design levels have beensuggestedinvariousstructures[6],[7].Br okenarraymultiplierwasdesignedforefficien tVLSIimplementation[8]. The error of mean and variance of the imprecise model increase by only0.63%and0.86%withreverencetothepre ciseWPAandthemaximumerrorincreasesby 4%.Low-Power DSP uses approximate adders which are employed in different algorithms anddesign for signal processing. In contrast with standard multiplier, the dissipated power for theETMdroppedfrom75%to90%.Whilemai ntainingtheloweraverageerrorfromtheconv entionalmethod,theproposedETMachieves animpressivesavingsofmorethan50%fora 12 x 12 fixed-width multiplication. The crucial part of the arithmetic units are basically built by the multiplier hardware, so multipliers play a prominent role in any design. [1] If we consider a Digital signal processing (DSP) the internal blocks of arithmetic logic designs, where multiplier plays a major role among other operations in the DSP systems [1].So, in the design of multiplier and accumulate unit (MAC) multipliers play an important role. Next, important design in the MAC unit is the Adder. Adders also share the equal important in this design. By the appropriate function methods different kinds of adders and multipliers designs are been suggested. By the approximate computing the designer can make trade offs, accuracy, speed, energy and power consumption. In this paper we proposed the modified form ofroundingbasedapproximatemultiplierwhi chislowpowerdesign, highspeedandenergy

PROPOSEDSYSTEM

Existing system Drawbacks

1) More Number of Gates are required
2) It consumes more Power
3) More Complexity
4) Required more Hardware Components
5) Less Speed

recently proposed approximate Booth encoder is based on four Booth-encoded

signals (s, ×1, ×2 and ×4); however, by mapping this encoder to FPGAs, performance is not improved, because it still requires two LUTs for its implementation, same as required in theexactradix-8encoder

Thegenerationofthe×4encodedsignalinanexactradix-8encoderisacomplex operation as it requires two XOR gates (2-input), one XNOR gate (2-input) and oneOR gate (3-input). This complexity can be reduced by using small approximation in theencoder.Thepartialproductsagainstthein puts{(0000)and(1111)}areapproximatedm ultiplicand can easily be generated by XNOring ×1 and ×2, so there is no need to separatelygeneratethe×4encodedsignal(Ta ble).InAxE1,theabsolutevalueoftheapproxi mateproductisgreater than the exact counterpart,3C are approximated to}4C multiplicands. AxE2 isdesigned such that for a specific logic circuit, positive and negative errors complement eachother. Thus, the positive 3C multiplicand is approximated to 4C whereas the negative 3Cmultiplicandisapproximatedto2C

LITERATURE SURVEY

A traditional method to reduce the aging effects is overdesign which includes techniques likeguard-banding ad gate oversizing. This approach can be area and power inefficient [8]. To avoidthisproblem,anNBTI-awaretechnologymappingtechnique waswproposedin[7]whichguarantee the performance of the circuit during its lifetime. Another technique was an NBTI-aware sleep transistor in [3] which improve thelifetime stability of the power gated circuitsunder considerations. A joint logic restructuring and pin reordering method in [6] is based ondetectingfunctionalsymmetriesandtransi storstackingeffects.ThisapproachisanNBTI optimization method that considered path sensitization. Dynamic voltage scaling andbogy-biasing techniques were proposed in [4] and [5] to reduce power or extend circuit life. Thesetechniques require circuit modification or do not provide optimization of specific circuits. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. However, in many worst-case designs, the probability that the critical path delay is activated is low. In such cases, the strategy of minimizing the worst-case conditions may lead to inefficient designs. Form on critical path, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable latency design was proposed to reduce the timing waste of traditional circuits. A short path activation function algorithm

waspropose din[16]toimprovetheaccuracyo ftheholdlogicandtooptimizetheperformance ofthevariable-latencycircuit.

An instruction scheduling algorithm was proposed in [17] to schedule the operations onnonuniform latency functional units and improve the performance of Very Long InstructionWordprocessors.In[18],avariabl e-latency pipelinedmultiplier architecturewithaBoothalgorithm was proposed.

RELATED WORK

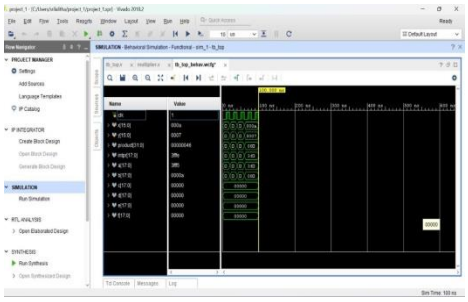
Booth's Multiplication Algorithm is a Multiplication algorithm that multiplies two signed binary numbers in two's complement notation. The algorithm wasinventedbyAndrewDonaldBoothin195 0whiledoingresearchoncrystallographyatBi rkbeckcollegeinBloomsbury,London.

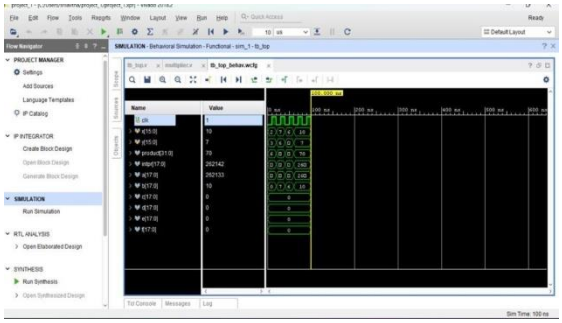
Booth used desk calculators that were faster at shifting than adding and created the algorithm to increase their speed. Booth's algorithm is of interest in the study of computer architecture.

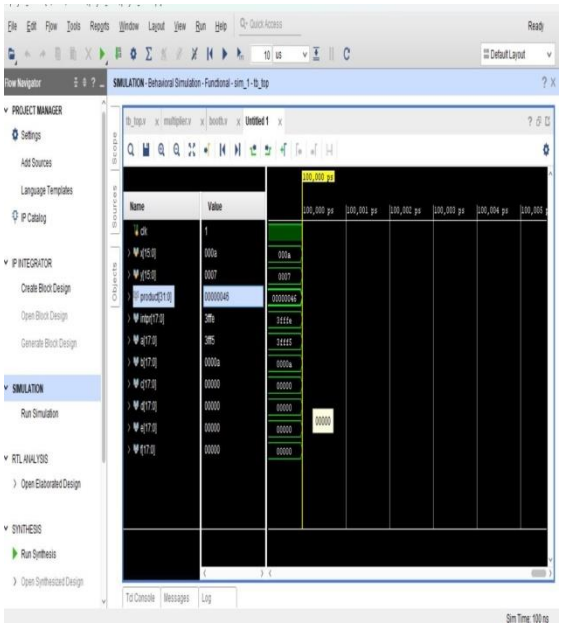
Vivado "projects" are directory structures that contain all the files needed by a particulardesign.Someofthesefilesareuser-createdsourcefilesthatdescribeandconstrain thedesign,but many others are system files created by Vivado to manage the design, simulation, andimplementation of projects. In a typical design, you will only be concerned with the user-created source files. But, in the future, if you need more information about your design, or ifyou need more precise control over certain implementation details, you can access the otherfilesas well.

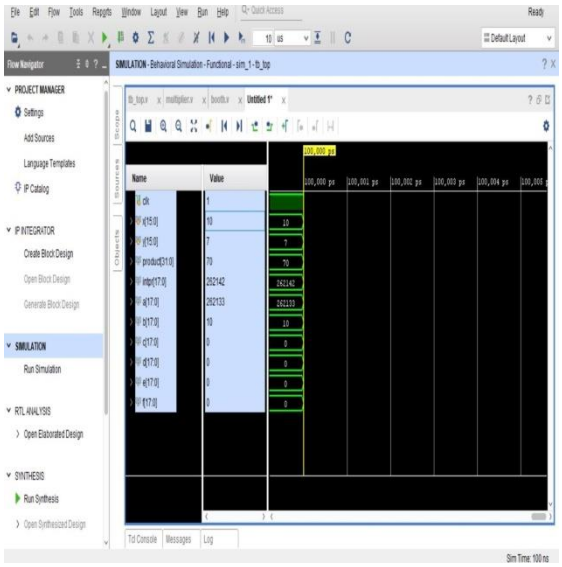
Verilog is a Hardware Description Language; a textual format for describing electroniccircuits and systems. Applied to electronic design, Verilog is intended to be used for circuitverification and simulation, for timing analysis, for test analysis (testability analysis and faultgrading)and for logic synthesis.

SAMPLE RESULTS









CONCLUSION

Finally, this project designs an approximate radix-8 Booth multiplier for FPGA-basedsystems has been studied. Efficient approximate design AxBM2 based on approximate Boothencodershavebeenimplemented.Asan extensionRadix-8modifiedboothencodingwithcarryskip addition algorithm is proposed for efficient implementation of multiplier. The proposedapproximation reduces the hardware for the Booth-encoded signals and lead to a design of asimplerpartialproductgeneratorwhichiseffi cientlymappedusingasinglehardwarearchite cture.

REFERENCES

- W. Liu, F. Lombardi, and M. Shulte, “A retrospective and prospective view ofapproximate computing [point of view],” Proc. IEEE, vol. 108, no. 3, pp. 394–399, Mar.2020.
- H. Pettenghi, F. Pratas, and L. Sousa, “Method for designing efficient mixed radixmultipliers,”CircuitsSyst.Sign alProcess.,vol.33,no. 10,pp.3165–3193, 2014.
- W. Liu et al., “Design and analysis of approximate redundant binary multipliers,” IEEETrans. Comput., vol. 68, no. 6, pp. 804–819, Jun.2019.

- S. Ullah, S. S. Murthy, and A. Kumar, "SMApproxLib: Library of FPGA-basedapproximate multipliers," in Proc. 55th Annu. Design Autom. Conf. (DAC), San Francisco,CA,USA, 2018, pp. 1–6.
- KuonandJ.Rose,"Measuringthegap between FPGAsandASICs,"IEEETrans.Co mput.-AidedDesignIntegr.CircuitsSyst., vol.26,no.2,pp.203–215,Feb.2007.
- M. Kumm, S. Abbas, and P. Zipf, "An efficient softcore multiplier architecture for XilinxFPGAs,"inProc.22ndSymp.C omput.Arithmetic(ARITH), Lyon,France,2015,pp.18–25.
- M. Langhammer and G. Baeckler, "High density and performance multiplication forFPGA," in Proc. 25th Symp. Comput. Arithmetic (ARITH), Amherst, MA, USA, 2018, pp.5–12.
- Y. Guo, H. Sun, and S. Kimura, "Small-area and low-power FPGAbased multipliers usingapproximate elementary modules," in Proc. 25th Asia South Pac. Design Autom. Conf. (ASP-DAC),Beijing, China, 2020,pp. 599–604.
- Z. Ebrahimi, S. Ullah, and A. Kumar, "LeAp: Leading-one detectionbased softcoreapproximate multipliers with tunable accuracy," in Proc. 25th Asia South Pac. DesignAutom.Conf. (ASP-DAC), Beijing, China, 2020, pp. 605–610.
- N. Van Toan and J. Lee, "FPGA-based multi-level approximate multipliers for high-performanceerror-resilient applications,"IEEEAccess,vol.8,pp. 25481–25497,2020.