A NOVEL APPROACH SYNCHRONOUS BINARY COUNTER WITH MINIMAL CLOCK

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ABSTRACT: A synchronous binary counter is a fundamental component in VLSI design which are used commonly. synchronous binary counter is fast and are used in many applications as it supports wide bit-width. Due to large fan-outs and long carry chains many previous counters have low counting rate when the size of the counters is large. In this article, we present a novelmethod of fast saturated binary counters based on the sorting network. The inputs of the counter are asymmetrically divided into two groups and fed into sorting networks to generate reordered sequences, which can be solely representedby one-hot code sequences. Between the reordered sequence and the one-hot code sequence, three special Boolean equations are established, which can significantly simplify the output Boolean expressions of the counter. Further, this project is enhanced by using parallel sorting algorithms for finding/ sorting M largest values from N inputs and then design scalable architectures based on proposed algorithms. For finding the largest values the iterative sorting techniques also proposed. MINMAXC SORTING is one type of efficient such algorithm for implementing with optimized parameters.

KEYWORDS-Backwardcarry propagation, binary counter, constant-time counter, prescaled counter

INTRODUCTION

Energy minimization is major requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets. It is extremely desired to attain this minimization with minimal performance (speed) penalty. Digital signal processing (DSP) blocks are most wanted in transportable components for realizing various multimedia applications.

The computational core of these blocks is the ALU where the multiplications and additions are the major part. The multiplications play foremost operation in the processing elements which can leads to high consumption of energy and power.

Many of the DSP cores implement image and video processing algorithms where final outputs are either images or videos prepared for human consumptions.

It facilitates to go for approximations for improving the speed and energy in the arithmetic circuits. This originates from the limited perceptual abilities in observing an image or a video for human beings. In addition to the image and video processing applications, there are other areas where the exactness of the arithmeticoperations is not critical to the functionality of the system. Approximate computing provides an accuracy, speed, and power/energy consumption. The advantage of approximate multiplier reduces the error rate and gain high speed. For correcting the division error compare operation and a memory look up is required for each operand is required which increases the time delay for entire multiplication process. At various level of abstraction including circuit, logic and architecture levels the approximation is processed.

In the category for approximation methods in function, a numberof approximating arithmetic building blocks, such as adders and multipliers, at different designlevels have been suggested in various structures. Broken array multiplier was designed forefficient VLSI implementation.

PROPOSEDSYSTEM

Existing system Drawbacks

In the realm of electronic circuits, digital counters play a pivotal role in various applications, from basic counting tasks to more complex sequencing and timing functions. This report aims to explore the functionality, types, and applications of digital counters, along with their significance in electronic design.

High-Speed Data Processing: In areas like telecommunications or internet infrastructure, you need to process vast amounts of data rapidly. Fast binary counters help keep track of data packets or requests, while sorting networks ensure the data is in the right order for further processing.

Computer Graphics: When rendering complex scenes, computers often need to sort visual elements quickly. Sorting networks can help organize these elements efficiently, ensuring that the final image is composed correctly and swiftly.

Financial Markets: Trading platforms deal with thousands of transactions and bids per second. Fast binary counters can track these transactions, and sorting networks can helpin ordering them by price or time, making sure the market operates smoothly and fairly.

Big Data and Analytics: Analyzing large datasets to find patterns or insights requires sorting through massive amounts of information. Fast binary counters and sorting networks can speed up this process, making it feasible to analyse big data in real-time.

Embedded Systems and IoT Devices: In devices like smart sensors, you need to process and sort data quickly using minimal power. These technologies offer efficient ways to handle data in constrained environments.

LITERATURE SURVEY

A traditional method to reduce the aging effects is overdesign which includes techniques like guard-banding ad gate oversizing. This approach can be area and power inefficient. To avoid this problem, an NBTI- aware technology mapping technique was proposed in which guarantee the performance of the circuit during its lifetime. Another technique was an NBTI-aware sleep transistor in which improve the lifetime stability of the power gated circuits under considerations.A joint logic restructuring and pin reordering method in is based on detecting functionalsymmetries and transistor stacking effects. This approach is an NBTI optimization method that considered path sensitization. Dynamic voltage scaling and bogy-biasing techniques were proposed in and to reduce power or extend circuit life. These techniques require circuit modification or do not provide optimization of specific circuits.

Every gate in any VLSI circuit has its own delay which reduces the performance of the chip. Traditional circuits use critical path delays the overall circuit clock cycle to perform correctly. However, in many worst-case designs, the pMRSAbility that the critical path delay is activated is low. In such cases, the strategy of minimizing the worst-case conditions may lead to inefficient designs. For noncritical path, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable latency design was proposed to reduce the timing waste of traditional circuits. A short path activation function algorithm was proposed in to improve the accuracy of the hold logic and to optimize the performance of the variable-latency circuit. An instruction scheduling algorithm was proposed in to schedule the operations on nonuniform latency functional units and improve the performance of Very Long Instruction Word processors. In a variable-latency pipelined multiplier architecture with a Booth algorithm was proposed. In process-variation tolerant architecture for arithmetic units was proposed, where the effect of process-variation is considered to increase the circuit yield. In addition, the criticalpaths are divided into two shorter paths that could be unequal and the clock cycle is set to the delay of the longer one.

RELATED WORK

Simple sorts**:**

Two of the simplest sorts are insertion sort and selection sort, both of which are efficient on small data, due to low overhead, but not efficient on large data. Insertion sort is generally faster than selection sort

in practice, due to fewer comparisons and good performance on almost-sorted data, and thus is preferred in practice, but selection sort uses fewer writes, and thus is used when write performance is a limiting factor.

Insertion sort

Insertion sort is a simple sorting algorithm that is relatively efficient for small lists and mostly sorted lists, and often is used as part of more sophisticated algorithms. It works by taking elements from the list oneby one and inserting them in their correct position into a newsorted list. In arrays, thenew list and the remaining elements can share the array's space, but insertion is expensive, requiring shifting all following elements over by one. Shell sort (see below) is a variant of insertion sort that is more efficient for larger lists.

Selection sort:

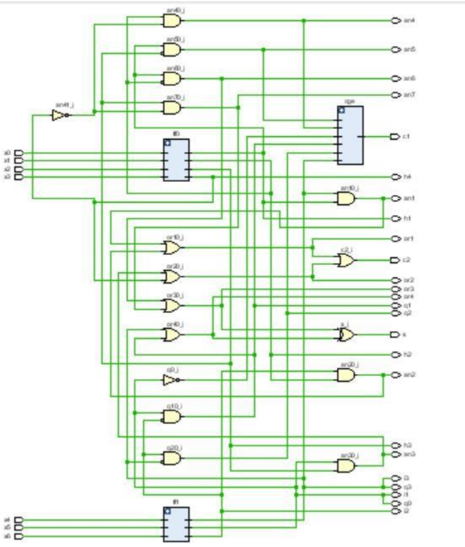
Selection sort is an in-place comparison sort. It has O(n^2) complexity, making it inefficient on large lists, and generally performs worse than the similar insertion sort. Selection sort is noted for its simplicity, and also has performance advantages over more complicated algorithms in certain situations.

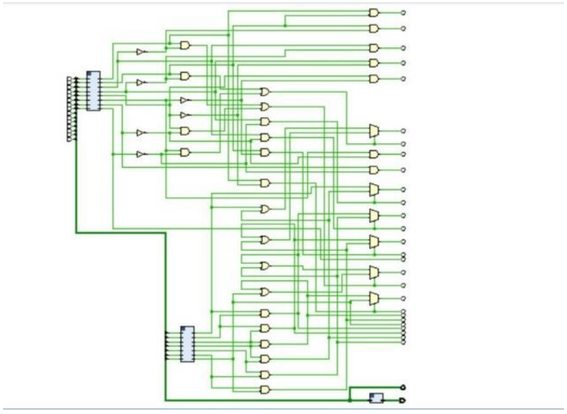
The algorithm finds the minimum value, swaps it with the value in the first position, and repeats these steps for the remainder of the list. It does no more than *n* swaps, and thus is useful where swapping is very expensive.

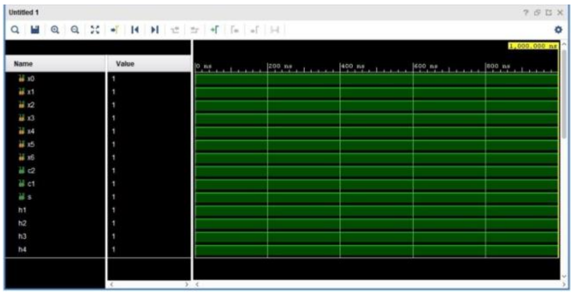
Efficient sorts**:**

Practical general sorting algorithms are almost always based on an algorithm with average complexity (and generally worst-case complexity) O(*n* log *n*), of which the most common are heap sort, merge sort, and quicksort. Each has advantages and drawbacks, with the most significant being that simple implementation of merge sort uses O(*n*) additional space, and simple implementation of quicksort has O(n^2) worst-case complexity. These problems canbe solved or ameliorated at the cost of a more complex algorithm.

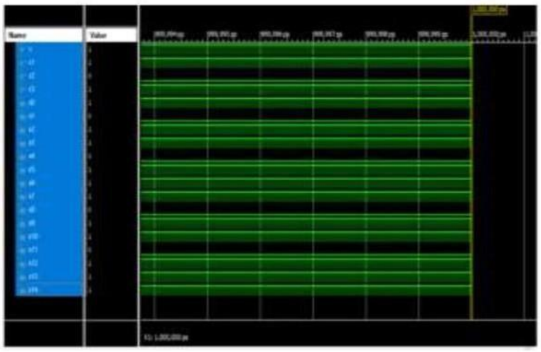
SAMPLE RESULTS

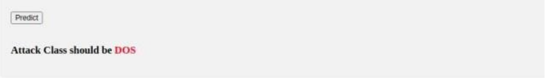






Name	Value
x0	1
x1	1
x2	1
x3	1
x4	1
x5	1
x6	1
c2	1
c1	1
s	1
h1	1
h2	1
h3	1
h4	1





Attack Class should be DOS

CONCLUSION

In this paper, a plan strategy for region viable and speed effective counter is planned and reproduced. A twofold counter in view of a novel symmetric piece Aggregate and convey computation approach is proposed. In this process, a new counter design method based on a sorting network is proposed, and we construct (7,3), (15,4) counters based on this min max sorting method. Proposed counters are more flexible than existing designs because it achieves less delay when the speed is critical and performs in better in ADP

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