IMPLEMENTATION OF REGISTER REUSING FOR LOW POWER AND AREA EFFICIENT SHIFT REGISTER

SRIRAM SONIYA SREE*, DR.T. ANIL KUMAR, DR.K. NIRANJAN REDDY*****

PG SCHOLAR*, PROFESSOR, HOD& PROFESSOR*****

DEPARTMENT OF ECE, CMR INSTITUTE OF TECHNOLOGY KANDLAKOYA VILLAGE, MEDCHAL ROAD, HYDERABAD, TELANGANA ,501401

ABSTRACT:

This process solves the timing problem between pulsed latches by using multiple non-overlap postponed pulsed clock signals rather than the traditional single pulsed clock signal. This paper proposes a minimal-power and area-efficient shift register using pulsed latches. The architecture of the shift register is very simple. An N-bit shift register consists of series connected N data switch-flops. The rate from the switch-flop is less important compared to area and power consumption because there's no circuit between switch-flicks within the shift register. The region and power consumption are reduced by changing switch-flops with pulsed latches. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using CMOS process with. The suggested shift register saves area and power in comparison towards the conventional shift register with switch-flops. Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop. However the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches.

Keywords: Area-efficient, flip-flop, pulsed clock, pulsed latch, shift register.

I. INTRODUCTION

Lately, as how big the look data is constantly on the increase because of the popular for prime quality image data, the term entire shifter register increases to process large image data in image processing ICs. A picture-extraction and vector generation VLSI nick utilizes a 4K-bit shift register. A Ten-bit 208 funnel output LCD column driver IC utilizes a 2K-bit shift register. A shift register may be the fundamental foundation inside a VLSI circuit. Shift registers are generally utilized in many programs, for

example digital filters, communication receivers, and image processing ICs [1]. A 16-megapixel CMOS image sensor utilizes a 45K-bit shift register. Because the word entire shifter register increases, the region and power use of the shift register become important design factors. The architecture of the shift register is very simple. An N-bit shift register consists of series connected N data switch-flops. The rate from the switch-flop is less important compared to area and power consumption because there's no circuit between switch-flicks within the shift register. The tiniest switch-flop is appropriate for that shift register to lessen the region and power consumption. Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop [2]. However the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches. This paper proposes a minimal-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap postponed pulsed clock signals rather than the traditional single pulsed clock signal. The shift register uses a small amount of the pulsed clock signals by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches. Another option would be to insert clock buffers and clock trees to transmit rapid clock pulse having a small wire delay. However this boosts the area and power overhead.

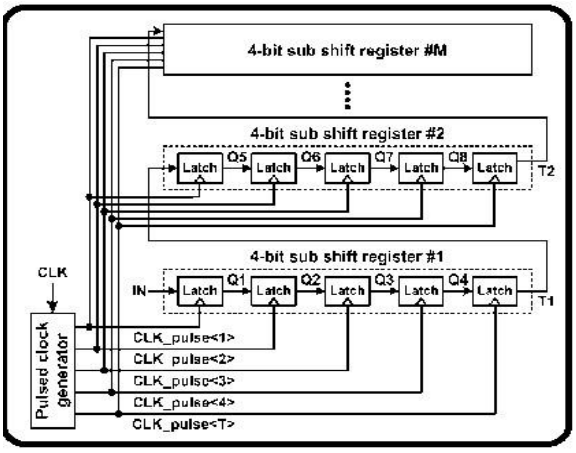

Fig.1.Block diagram of proposed shift register

II. PROPOSED METHOD

An expert-slave switch-flop using two latches could be changed with a pulsed latch composed of the latch along with a pulsed clock signal. All pulsed latches share the heart beat generation circuit for that pulsed clock signal. Consequently, the region and power use of the pulsed latch become nearly half of individuals from the master-slave switch-flop [3]. The pulsed latch is definitely an attractive solution for small area and occasional power consumption. The pulsed latch can't be utilized in shift registers because of the timing problem. The shift register includes several latches along with a pulsed clock signal (CLK_pulse). The operation waveforms are definitely the timing issue in the shifter register. The output signal

from the first latch (Q1) changes properly since the input signal from the first latch (IN) is constant throughout the clock pulse width. However the second latch comes with an uncertain output signal (Q2) because its input signal (Q1) changes throughout the clock pulse width. One solution for that timing issue is to include delay circuits between latches. The output signal from the latch is postponed and reaches the following latch following the clock pulse. The output signals of the foremost and second latches (Q1 and Q2) change throughout the clock pulse width , however the input signals from the second and third latches (D2 and D3) become identical to the output signals of the foremost and second latches (Q1 and Q2) following the clock pulse. Consequently, all latches have constant input signals throughout the clock pulse with no timing problem happens between your latches. However, the delay circuits cause large area and power overheads. Another solution is by using multiple non-overlap postponed pulsed clock signals. The postponed pulsed clock signals are produced whenever a pulsed clock signal experiences delay circuits. Each latch utilizes a pulsed clock signal that is postponed in the pulsed clock signal utilized in its next latch. Therefore, each latch updates the information after its next latch updates the information. Consequently, each latch includes a constant input during its clock pulse with no timing problem happens between latches. However, this solution also requires many delay circuits. Inside a lengthy shift register, a brief clock pulse cannot via a lengthy wire because of parasitic capacitance and resistance. In the finish from the wire, the time pulse shape is degraded since the rising and falling occasions from the clock pulse increase because of the wire delay. An easy option would be to improve the time pulse width to keep the time pulse shape [4]. However this lessens the maximum clock frequency. Another option would be to insert clock buffers and clock trees to transmit rapid clock pulse having a small wire delay. However this boosts the area and power overhead. Furthermore, the multiple clock pulses result in the more overhead for multiple clock buffers and clock trees. The utmost clock frequency within the conventional shift register is restricted to simply the delay of switch-flops because there's no delay between switch-flicks. Therefore, the region and power consumption tend to be more important compared to speed for choosing the switch-flop. The suggested shift register uses latches rather than switch-flops to lessen the region and power consumption. In nick implementation, the SSASPL, the tiniest latch, is chosen. The initial SSASPL with 9 transistors is modified towards the SSASPL with 7 transistors by getting rid of an inverter to create the complementary data

input (Db.) in the data input (D). Within the suggested shift register, the differential data inputs (D and Db.) from the latch range from differential data outputs (Q and Qi) from the previous latch [5]. The SSASPL uses the tiniest quantity of transistors (7 transistors) also it consumes the cheapest clock power because it features a single transistor driven through the pulsed clock signal. The SSASPL updates the information with three NMOS transistors also it supports the data with four transistors in 2 mix-combined inverters.

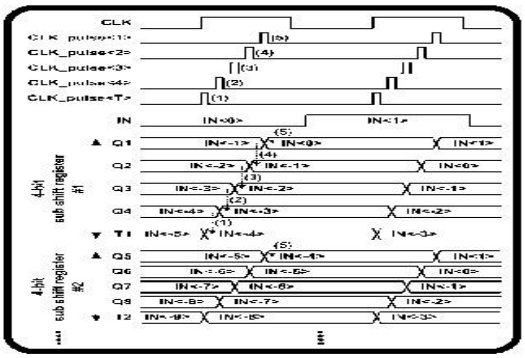

Fig.2.Proposed shift register waveform

CIRCUIT DIAGRAM:

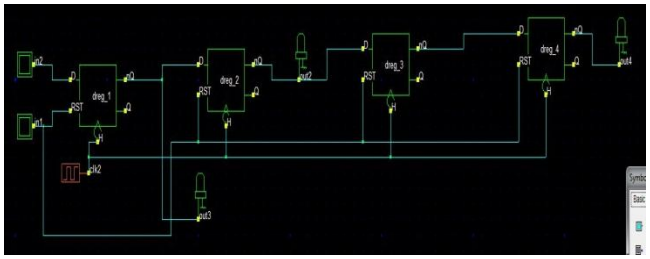

Fig : Pulsed Latch Circuit

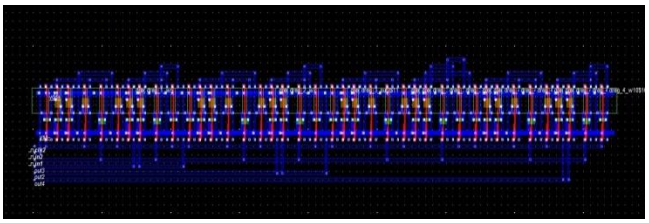

Fig : Lay Out

Fig: Result Wave Forms

RTL SCHEMATIC

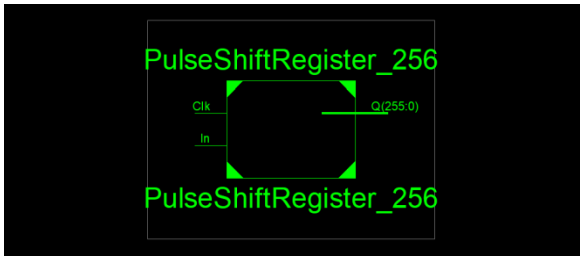

Fig pulsed shift register

PULSED GENERATOR

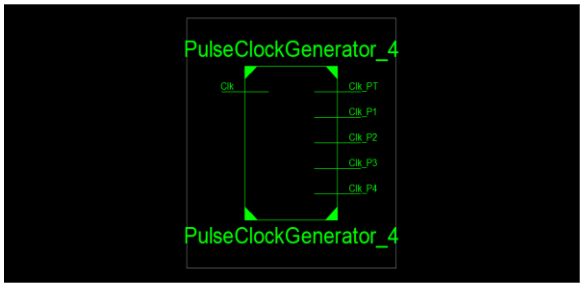

Fig pulsed generator

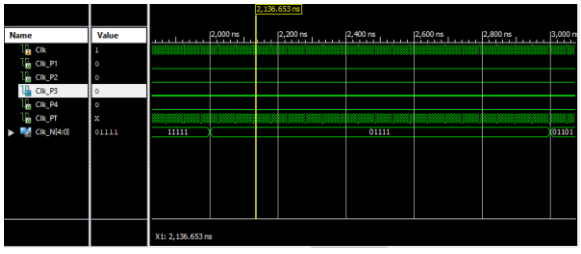

Fig Simulation results

AREA REPORT

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Device utilization summary:
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Selected Device : 4vfx12sf363-12

 Number of Slices:                        0  out of   5472     0%
 Number of IOs:                           6
 Number of bonded IOBs:                   5  out of    240     2%
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Fig Area Report

TIMING REPORT

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Timing Summary:
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Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: No path found

Timing Detail:
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All values displayed in nanoseconds (ns)

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Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.62 secs

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```

Fig Timing report

POWER REPORT

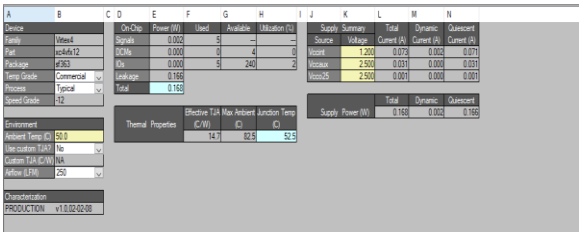

Fig Power Report

IV. CONCLUSION

Lately, pulsed latches have changed switch-flops in lots of programs, just because a pulsed latch is a lot smaller sized than the usual switch-flop. However the pulsed latch can't be utilized in a shift register because of the timing problem between pulsed latches. . A 256-bit shift register was fabricated utilizing a .18 CMOS process with. It consumes 1.2 maw in a 100 MHz clock frequency. This paper suggested a minimal-power and area-efficient shift register using pulsed latches. The suggested shift register saves 37% area and 44% power in comparison towards the conventional shift register with switch-flops. The shift register reduces area and power consumption by changing switch-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap postponed pulsed clock signals rather than just one pulsed clock signal. A small amount of the pulsed clock signals can be used by grouping the latches to many sub shifter registers and taking advantage of additional temporary storage latches.

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