DESIGN AND IMPLEMENTATION OF HIGH-SPEED CARRY SELECT ADDER

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ABSTRACT: In electronic adder is a digital circuit that performs addition of numbers. Adders can be constructed for many numerical representations such as arithmetic and logical operation. The most adders operates on binary numbers. Among the different types of adders, carry select adder is a one of the fastest adder.The gate level modification is to reduce the power and area of carry select adder by using the concept of Arithmetic Logic Unit (ALU). In this paper , different techniques such as Binary To Excess Convertor (BEC), Common Boolean Logic (CBL) are implemented in Carry Select Adder(CSLA). On comparing these techniques ,the result analysis shows that proposed ALU is consumes less power and area than conventional CSLA.

KEYWORDS— Adder, Carry select adder (CSLA), Arithmetic Logic Unit (ALU), Common Boolean Logic (CBL).

I. INTRODUCTION Power consumption is an important efficiency factor in designing very large scale integrated (VLSI) circuit. Moreover with the explosive growth of VLSI technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area. The central electronic circuit used for addition is adder. Adders are fundamental for wide variety of digital system. Many adders exist but the fast adding with Low area and Power still challenging. There are different types of adders such as Ripple carry adder (RCA),carry skip adder (CSKA), carry look ahead adder (CLA), carry save adder (CSLA), etc. among them RCA shows compact design but their computation time is longer. It has lowest speed amongst all adder because it has large propagation delay but occupy less area. Then , in CLA can derive fast result but it leads to increase in area , among these adders CSLA have small area but delay is increased due to ripple carry adder. We have designed an efficient logic design for CSLA.

II. IMPLEMENTAION IN CARRY SELECT ADDER

A. carry select adder(csla) CSLA use multiple narrow adders to create fast wide adders. A CSLA breaks the addition problem into smaller groups. It is one of the fast type of adder.The adder consists of two independent units. Each unit implements the addition operation in parallel. One way to speed up the addition into several smaller groups ,with each having N-bit, say 8-bit groups and then for

each group four additions are performed in parallel, one assume carry in is‟ 0‟(CIN=0) and the other assuming the carry in is „1‟ (CIN=1) .when the carry in is eventually known the correct sum is simply selected through a N-bit using 2-to-1 mux. The adder based on this approach is known as carry select adder (CSLA).The application CSLA is used in data processing processor to perform fast arithmetic function.

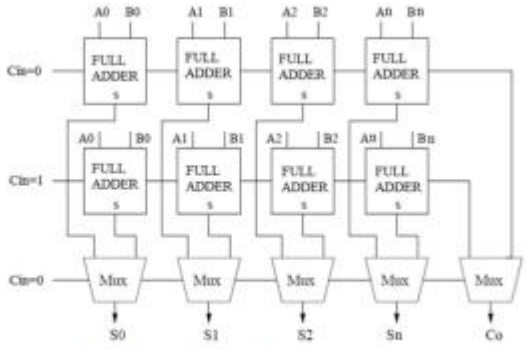

Fig:1 carry select adder

The gate count of 4- bit CSLA is ,

Gate Count=136(FA+MUX)

Full adder=104(13*8)

Mux=32(4*8)

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform, or variable. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays..

B. BEC BASED CSLA In this csla, the RCA which assume carry in is „1‟ is replaced using the BEC (BINARY TO EXCESS-1 CONVERTOR).In this the every full adder cell in RCA is wait for every carry in then the carry out is generated. Then to get linear dependency is to anticipate both possible values of carry in and evaluate the result for both possibilities in advance. Once the correct value of carry in is known the correct value is selected using multiplexer.

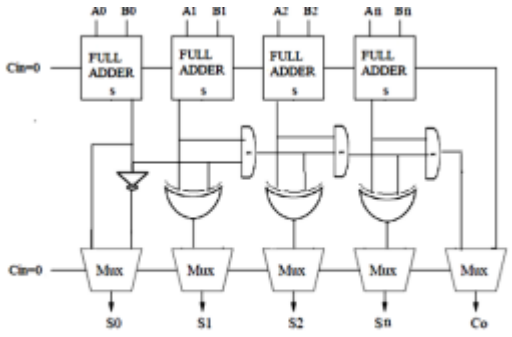

Fig:2 Binary-to-excess-1 convertor

The gate count of 4- bit BEC is ,

GATECOUNT=92 (FA+MUX+NOT+OR)

FA=52(13*4)

MUX=32(8*4)

NOT=4(4*1)

OR=4(1*4)

Instead of the RCA with cin 1 in order to reduce the area and power consumption of the regular CSLA. To replace the3-bit RCA, an 4-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig and the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1,and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

C. CBL BASED CSLA Boolean Logic was introduced in by George Boole in his first book The Mathematical Analysis of Logic (1847), and set forth more fully in his An Investigation Of Laws Thought (1854). According to Huntington the term "Boolean Logic" was first suggested by Sheffer in 1913.Boolean Logic has been fundamental in the development of digital electronics, and is provided for in all modern programming languages. In mathematics and mathematical logic, Boolean logic is the sub area of algebra in which the values of the variables in the truth table is as true and false, usually denoted as 1 and 0 respectively. Instead of elementary algebra where the values of the variables are numbers, and the important operations are addition and multiplication, the important operations of Boolean logic are the conjunction and, denoted ∧, the disjunction or, denoted ∨, and the negation not, denoted . It is thus a formalism for describing logical relations in the same way that ordinary Logic describes numeric relations. To share the common Boolean logic term, we only need to implement one XOR gate with one INV gate to generate the summation signal pair. As the carry-in signal is ready, we can select the correct summation output according to the logic state of carry-in signal. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance.

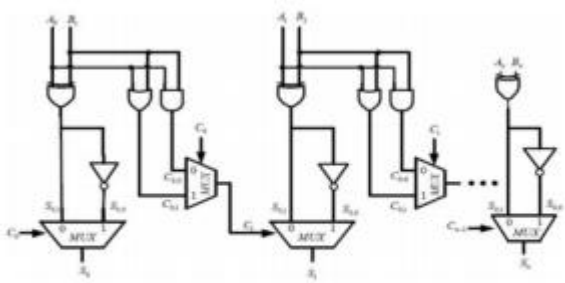

Fig:3 common boolean logic

The gate count of 4- bit CBL is,

GATECOUNT=88(FA+MUX+AND+NOT+EXOR)

FA=52(13*4)

MUX=20(5*4)

AND=3(3*1)

NOT=1(1*1)

EXOR=12(3*4)

Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal. In this way, we can keep both the summation generation circuit of XOR gate and INV gate and the carry-out generation circuit of OR gate and AND gate in parallel.

III. PROPOSED CSLA In this proposed adder we implementing the Csla in arithmetic and logic unit(ALU).the john von Neumann proposed the ALU concept. An ALU is a digital circuit that performs arithmetic and logic operation like addition, subtraction so on…ALU is building block of CPU. In digital electronics an ALU is a combinational circuit that performs arithmetic and bitwise logical operation on integer binary number. Many of the operation that we want to perform on group bits can be broken down into repeated operation on individual bits.

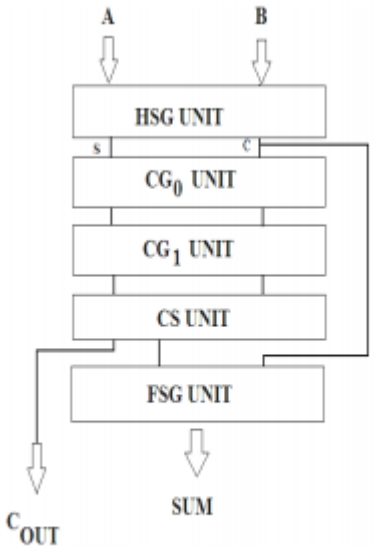

Fig:4 Arithmetic and logic unit

The gate used in the proposed CSLA are:

- The AND and EX-OR gate are used as Half Sum Generator (HSG).
- The OR and AND gate are used as Carry Generator (CG) and also in Carry Selector (CS).
- Then EX-OR is used as Full Sum Generator(FSG).

In this ALU consists of half sum generator (HSG), carry generator for Cin=0 (CG0), carry generator for Cin=1 (CG1), carry selector (CS) and full sum generator (FSG). The gate count of 4- bit ALU is ,

GATE COUNT =60(EXOR+AND+OR) E

XOR=8(8*2)

AND=16(16*1)

OR=12(12*1)

The proposed CSLA consists of is an HALF ADDER (HSG),which generate the sum(s0) and carry(C0).Then the C0 and S0 are passed through the carry generators ,which one assume carry in as„0"(CG0)and another assume carry in as „1"(CG1).The carry is selected by using carry selector(CS) with help of Cin. The full sum(FSG) is generator using the carry out (Cout) and half adder(S0).

ALGORITHM TO DESIGN ALU

1. Select the required operation to be performed by ALU.

2. At first required to built 1-bit ALU based on the concept "DIVIDE AND CONQUER".

3. The n-bit ALU can be sliced into n-equal part. This is called as "BIT SLICED METHOD".

4. In this bit slice approach, ALU is divided into arithmetic unit and logic unit.

CONCLUSION An efficient approach is planned in this paper to reduce the area and power of CSLA architecture. The reduced number of gates offers great advantage in the reduction of area and power. The compared result shows that the proposed CSLA has a low power and area consumption. The modified proposed CSLA architecture is having low area , low power and efficient for VLSI hardware implementation.

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