Implementation of Robust Low Power 12T SRAM Cell and Full Adder Using 180 nm,120 nm,90 nm, 70 nm & 50 nm Technologies

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ABSTRACT:

Static Random Access Memory(SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power. SRAM plays a most substantial .role in the microprocessor world but as the technology is scaling down in nanometers, leakage parameters and delay are the most common problems for SRAM cell which is basically designed for very low power application. The plan of different standard SRAM topologies with various technologies has been composed and tested for power dissipation as for the different technologies. For this thought distinct topologies viz 6T, 7T, 8T, 9T, 10T and 12T SRAM cells have been taken into considerations. These cells are designed using 120 nm,90 nm, 65nm and 45 nm technologies, The point by point investigation about these cells functionality and their characteristic behavior with the connected parameter of supply voltage is introduced. By utilizing DSCH software the results of power dissipation with respect to various technologies are determined. Likewise their layouts were designed using Microwind Software

Keywords: DSCH Software, Microwind Software

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1. INTRODUCTION

With the exceptional ascent of VLSI manufacturers have given increase in densities of integrated circuits by reducing gadget geometries in the course of past decades. These high density circuits has the drawback of powerlessness to power utilization despite the fact that they are giving high complexities. Likewise these circuits which consume more power has the inclination of run time disappointments for the dependability issues[1]. Major points impacting the need of low power configuration are expanding distinctive individualized computing devices viz. wireless communicating devices; smart cards, PDA's, digital pens , audio and video based multimedia products and so on particularly these devices and systems required rapid and complex designs and are constrained by the physical geometries of size and weight. They are mainly subject to battery lifetime. Among every one of these contemplations the primary concern is memory outline, which is a integral part of these devices. What's more, if decreasing of power dissipation for these systems is accomplished, advance in the system crucial parameters of reliability, execution and along performance and device efficiency[2] can achieve. As the SRAM cells are incorporated by latch, the refresh operation isn't required to keep the data during power on condition in SRAM cells.

Every one of the systems like microprocessors, hand held gadgets,

workstations have the cache memory which is outlined by SRAM cells due to its transistor favorable circumstances of giving quick exchanging and low power utilization. To store a single bit of data SRAM utilizes four transistors.

2. LITERATURE SURVEY

A. 6T SRAM:

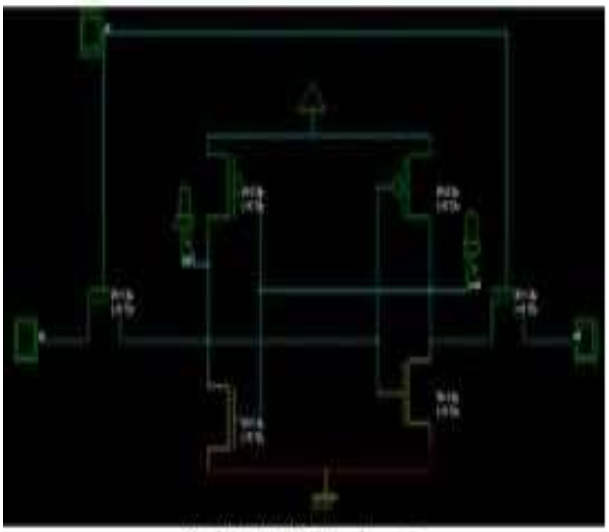


Fig 2.1: 6T SRAM schematic

During read pre-charge both bit lines to high at that point turn on word line. One of the two bit lines will be pulled down by the cell either BL (bit line genuine) or BLB (bit line complement) depending upon the stored data on internal nodes. A sense enhances changes over the strange signal to a logic-level output. At that point, toward the finish of the read task BL releases and BLB remains high.

During write activity the WL line goes high and the BL is forced to either the positive supply voltage VDD (depending upon the data) over driving the data of the memory cell. During hold state the WL is held low and BL and BLB are left floating or driven to VDD

B. 7T SRAM:

Both WL and BL signals are turned on while M5 is kept ON. At the point when BL node is '0' the read way comprises of M6 and M4 as appeared in Figure 2.2 and acts like a regular 6T cell. At the point when BL node is '1' the read way comprises of M2, M1 and M3 which represent to read way. In this basic side the three transistors are associated in series which helps in diminishing the driving capacity of the cell unless these transistors are precisely sizes. The write activity begins by turning M1 off to cut-off the functional bit connetion. BLB conveys compliment of the input data, M5 is turned on while M6 is kept off. The 7 SRAM cell looks like 2 cascaded inverters took after by inverter1. M5 transistor exchanges the

data from BLB to its node which drives second

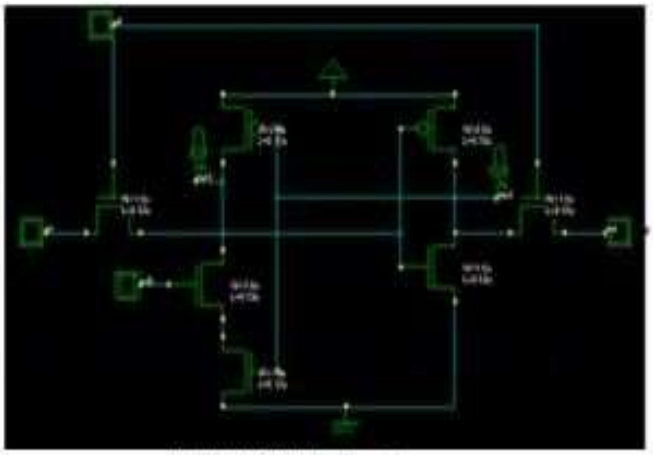


Fig2.2: 7T SRAM schematic

inverter, BL node and M4 to create BL node to the cell data. So also BL drives inverter 1, BL node1 and M2 to create compliment of BL node which approaches BBL node if data is '0' and marginally higher that BBL node if data is 1. The WL is turned off and M1 is turned on to reconnect the function bit interface between the two inverters to stable store the new data.

C. 8T SRAM:

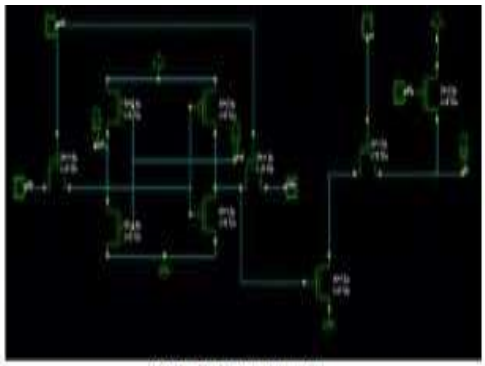


Fig2.3: 8T SRAM schematic

A dual port cell (8T-cell) is made by including two transistors. During read task gate of M7 was associated with node 1 and gate of M8 to node2. All things considered if Q='1' at that point BL will be released and node1='0', BLB will release. Along these lines, when the cell was storing logic '1' it gives lagic '0' at the output. To overcome these issue nodes M7 and M8 are interchanged.

D. 9T SRAM:

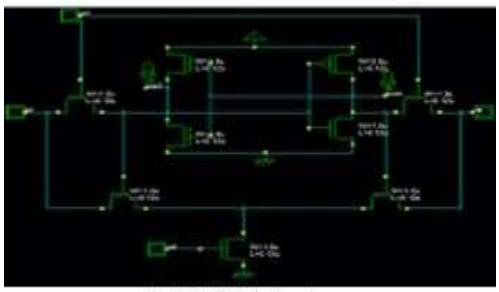


Fig2.4: 9T SRAM schematic

During write activity WL is high; M5 and M6 are equivalent to "1". N1 and N2 are the nodes of which gets to transistors M5 and M6. M9 is low and no input voltage is given to RD (M9). Subsequently exchanging M7 and M8 are low. In the event that there is any change in M9 then M7 and M8 likewise changes. To write "0" in the SRAM cell the bit lines BL and BLB are releasing and charging then "0" is constrained through SRAM cell through M3.Simultaneously,to make "0" in N2 bit lines BL and BLB are charging and releasing. During read task RD signal is high and WR is low. M9 will be in saturation, to store "1" in N1 the bit line BL is released through M7 and M9. To store "1", bit line BLB (M6) is released through M8 and M9. In the event that the transistors M5 and M6 are in cutoff mode N1 and N2 are totally isolated from the bit lines during read task.

E. 10T SRAM:

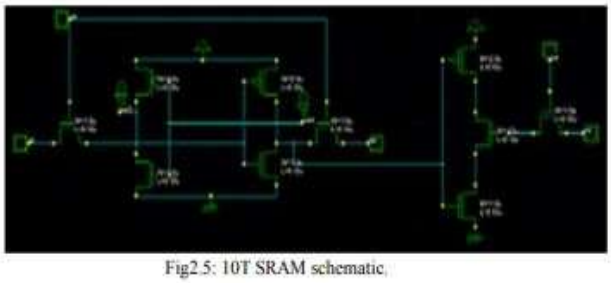


Fig2.5: 10T SRAM schematic

Figure 2.5 demonstrates the schematic of the 10T sub threshold bit cell. Write access to the bit cell happens through the write get to transistors. M5 and M6 transistors frame the write bit lines. Transistors M8 through M10 implent a buffer utilized for reading. Read get to is single finished and happens on a different bitline, RBL, which is pre-charged in before readed get to.

The word line for read is different from the write wordline. One key preferred standpoint by isolating the read and write word lines and bit lines is that a memory utilizing this bit cell can have different read and write ports.

3. PROPOSED METHOD

A. 12T SRAM

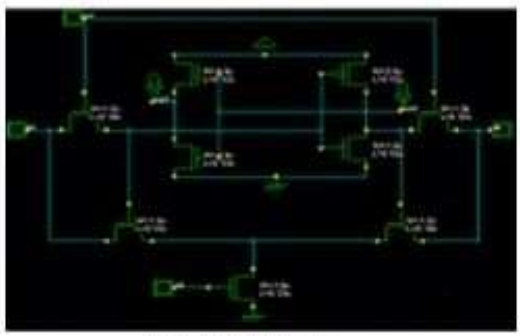


Fig2.4: 9T SRAM schematic

In the 12T SRAM when we high the WL=1 then the data passes through the M2,M11,M12 and WR the operation is out4 at high as well as the out3 at highWL=1;BL=1 and RD=1 then the trans coupling ON and data tranmission possible at out3. When the WL=1 and RD=1 then both coupling half of the transistors ON and data transfer to the out4 side. When the BL=1 then the data transmission is possible only cross coupled transistor then the out3 data is high at that time BL=1 and BLB=1 then M11 is open thandata possible at only one side than out3 high. The BLB=1 and WL=1 the data transmits only cross coupled transistor than out3 is high as well as BLB=0 and WL=1 the out3is only high because trans coupled system. When WL=1 and WR=1 then the output out4 is high i.e, WL=1 then it directcly transmit the data to M11 transistor as well as M12 as a WR=1 data. When WL=BL=RD=BLB=WR=1 then all data will be activated than the data transmitedd to the out3.When WL=BL=RD=BLB=WR=0 then the out3 is high. Here the data transmission possible only coupling transistor and supply.

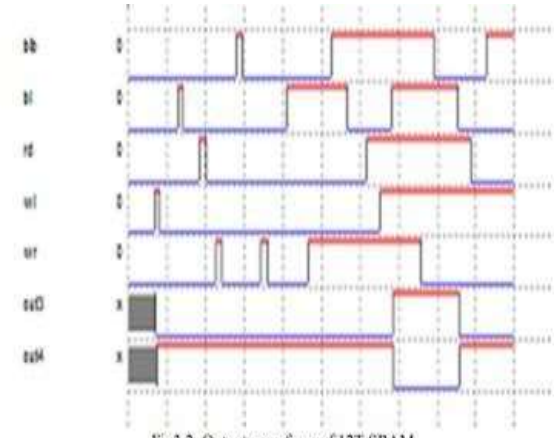


Fig3.2: Output waveform of 12T SRAM.

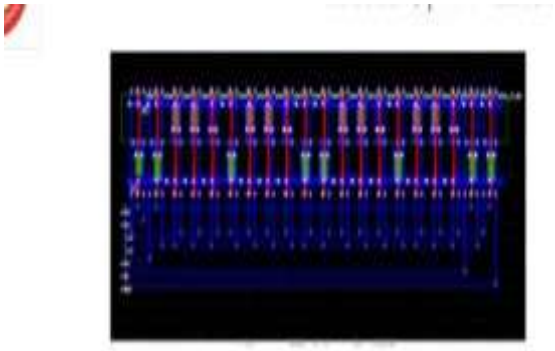


Fig3.3: Layout of 12T SRAM

The above figure shows the layout diagram of the 6T SRAM cell.

B. Full Adder using 12T SRAM cell

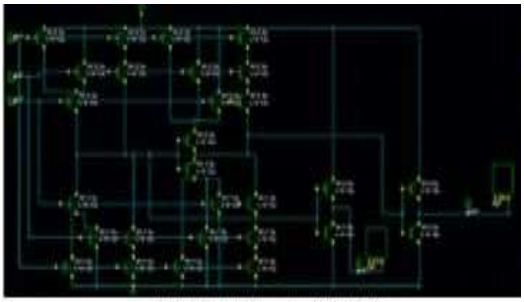


Fig3.4: Full Adder using 12T SRAM.

In the proposed system we are implimenting SRAM with 12T transistor as well as with one Full Adder circuit. It is a asynchronous circuit. In that circuit we are giving 3 inputs and calculate Sum and Carry at the output side and it denoted as out3,digit2 and out4, digit1. When we are applying in1=1 and in2=in3=0 then the data transmits through upper circuit and data should be high at out4 and digit1=1;as well as we are applying in1=in2=1 then the data transmitted through upper and lower circuit and produce the output at out3=1 and digit2=1 because it generated carry and that carry forwarded to next bit. We are applying all inputs are high i.e, 1 then data forwarded to upper and lower side and produce the output out3 and out4 side because when 3 input's high one full adder generated sum as well as carry so out3 and out4 are high.

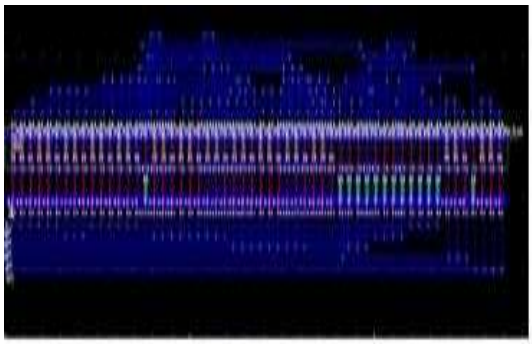


Fig3.6: Layout of Full Adder.

. SIMULATION RESULTS:

A. 120 nm Technology

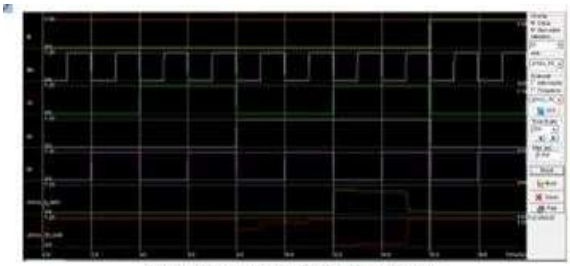
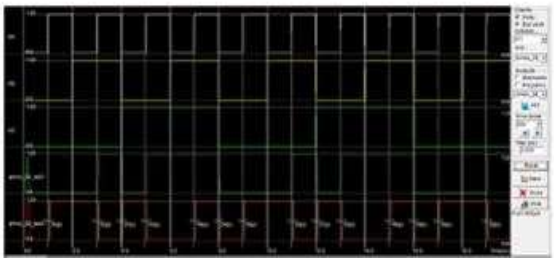


Fig4.1: Power consumption of 12T SRAM



B. 90 nm Technology

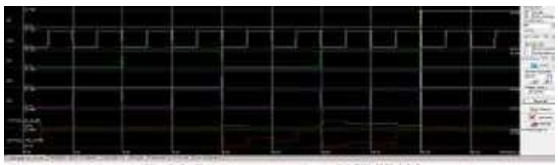


Fig4.5: Power consumption of 12T SRAM

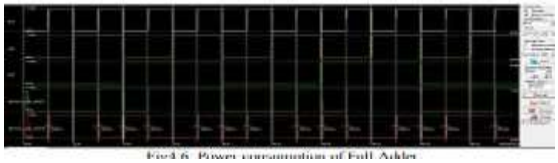


Fig4.6: Power consumption of Full Adder

B. 65 nm technology

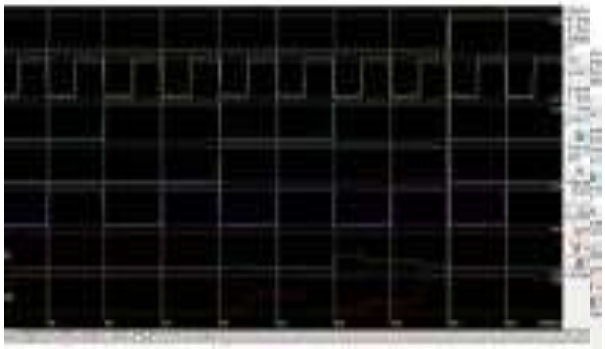


Fig4.5: Power consumption of 12T SRAM

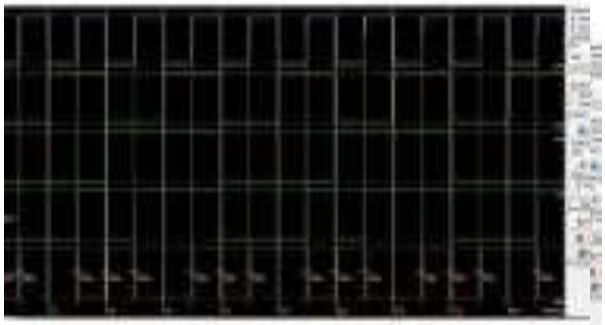


Fig4.6: Power consumption of Full Adder

Fig4.6: Power consumption of Full Adder

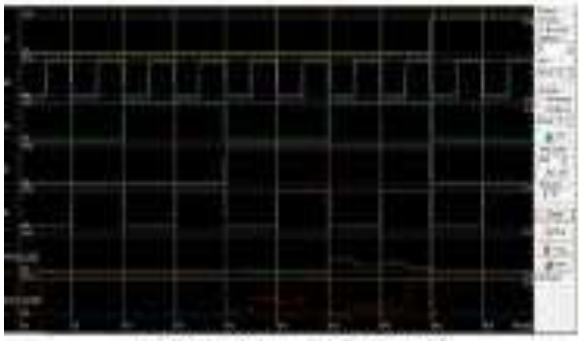
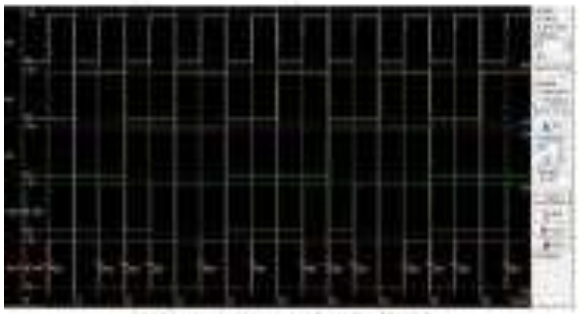
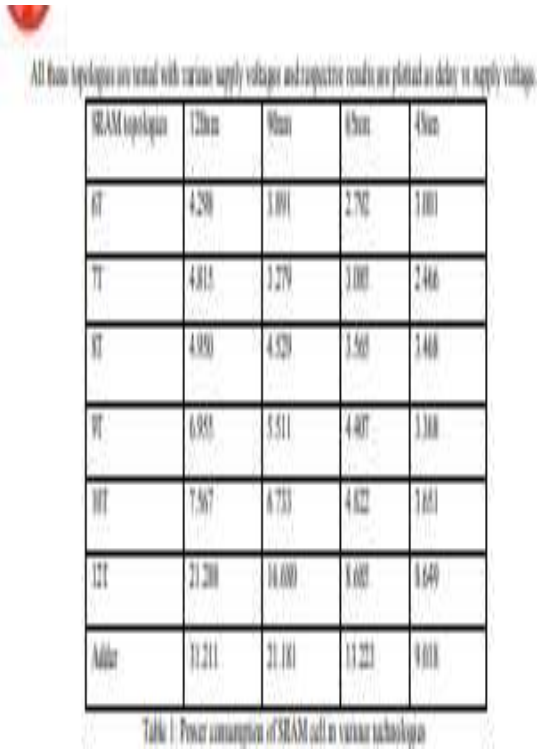


Fig4.7: Power consumption of 12T SRAM



C.

Fig4.8: Power consumption of Full Adder



All these topologies are tested with various supply voltages and respective results are plotted as shown in supply voltage

SRAM topologies	120nm	90nm	65nm	45nm
6T	4.298	1.891	2.702	1.003
7T	4.815	1.279	1.000	2.466
8T	4.950	4.529	3.560	3.468
9T	6.955	5.511	4.407	3.308
10T	7.567	6.733	4.522	3.651
12T	21.200	16.600	8.605	8.649
Adder	31.211	21.101	11.223	9.018

Table 1 Power consumption of SRAM cell in various technologies

5.. CONCLUSION

Some standard SRAM cells of 6T, 7T, 8T, 9T, 10T, 12T and Full Adder using 12T SRAM have taken and intended to test their behaviour and functionality with various technologies as for their benefits and bad marks. The detailed examination of these memory cells power consumption in various technologies of 120nm, 90nm, 65nm and 45nm technologies has talked about. And their layouts has additionally designed. For designing and simulation microwind software is used.

6. FUTURE SCOPE

This paper is limited to 45nm technology. Future work aims to more design for SRAM based under new technologies

6. REFERENCES

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