Design And Simulation Of A Low Power 4 - Bit Magnitude Comparator Circuit Using Cmos In Dsch And Microwind

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Abstract

In this project, we implemented a 4-bit comparator circuit at the Complementary Metal Oxide Semiconductor (CMOS) technology nodes of 90 nm, 65 nm, and 45 nm.At first, we designed a 4-bit magnitude comparator circuit in DSCH with 8 inputs and 3 outputs.After that, we created compilation codes for the Microwind tool to observe the layout diagram for the designed 4-bit comparator circuit.Then we obtain layout diagram, simulate the voltage vs. time diagram, obtain a 3-D view of the designed circuit, etc. using Microwind tool.We showed the basic operation of a 4-bit comparator circuit and generated the output characteristics curves and determined power dissipation of the circuit.Based on the performance comparisons at various nodes through the simulation results, revealed that the reduction of the technology nodes improves the circuit performance in terms of power dissipation.Reduction of the technology along with supply voltage scaling for different nodes improves the circuit performance.

Keywords: 4 - Bit Magnitude Comparator, (CMOS) technology nodes, power dissipation, supply voltage scaling.

I. Introduction:

A binary comparator circuit based on CMOS is one of the most significant modules of any digital structure and is widely used in computer-based systems. For example, it grips a central position in a fast Analog to Digital Converter (ADC) circuit to transform an analog signal into digital . The comparator is used to compare the magnitudes between two binary numbers each having the same number of bits to determine a relationship between them. If the number of bits in each number is four then it is called a 4-bit comparator. As such, it consists of eight inputs each for two 4- bit numbers. However, as the numbers of bits of the two comparing numbers are augmented, the occupying area, power supply requirement, and propagation delay of the circuit will also grow accordingly.

As such, to keep these operating parameters constant or even to diminish more, the transistor dimension is to be reduced. As a result, higher packing density and lower power supply, as well as propagation delay, can be achieved. CMOS is the most widely used technology due to its higher speed and packing density, as well as lower power consumption or dissipation. Moreover, its node can be scaled down to enhance the performance. Therefore, to design a compact 4-bit comparator circuit with improved performance, we have selected a CMOS transistor-based logic circuit to have a comparative picture of various performance parameters as its technology node is scaled down. The term technology node, process node, process technology, or just the node denotes a definite semiconductor device manufacturing method and its corresponding design guidelines. Usually, it means the value of the MOS transistor size. At present, the available technology nodes are 90 nm, 70 nm, 50 nmand so on .

Usually, the smaller-sized node means the most recent available technology. In this paper, we have reported the design process of a 4-bit comparator circuit, and have provided the simulation results at 3 CMOS technology nodes, like 90 nm, 70 nm, and 50 nm. We obtained improved performances in terms of surface area requirement, power dissipation, and propagation delay of the circuit at these three nodes. This article gives an overview of the comparator circuit design steps in DSCH and Micro wind.

II. Conventional 4-Bit Magnitude comparator

II.a. Comparator:

Comparing two words for equality is a commonly used operation in computer systems and device interfaces. A circuit that compares two binary words and indicates whether they are equal is called a comparator. Some comparator interpret

their input words as signed or unsigned numbers and also indicate an arithmetic relationship (greater or less than) between the words. These devices often called magnitude comparator.

Fig .1 : Logic diagram of comparator

II.a. Types Of Comparator:

There are two types of comparators . They are
1) Identity comparator
2) Magnitude comparator

1) Identity Comparator:

A digital comparator that compares only the equality of two applied signals at its inputs is known as identity comparator. It has 2 inputs and only 1 output pin. The output pin shows a logic high signal when the two values are equal otherwise it shows a low signal. More specifically, we can say, for two inputs P and Q, if P is equal to Q then output shows HIGH and if P is not equal to Q then output shows LOW.

2)Magnitude Comparator:

Basically a magnitude comparator makes the comparison by considering all the factors. It shows results for either greater, equal or lesser than value by comparing the magnitude of two inputs. Hence contains 3 output pins and accordingly, any one of the three output pins of a magnitude comparator becomes high. Suppose P and Q are the two inputs of magnitude comparator. And the 3 outputs will be P > Q, P = Q and P < Q. And depending upon the comparison performed, any one of the given outputs will be high. Magnitude comparator can be classified as follows:

a) 1-BIT MAGNITUDE COMPARATOR:

As we can see that for 2 binary input of 1-bit each, we are having 4 possible combinations. And therefore depending on the comparison performed on P and Q, the magnitude comparator makes high any one of the output pins among the three. It is clear from the truth table shown above that when both the inputs are same i.e., either 0 or 1, then pin 2nd which is showing equivalency between the two value in comparison becomes high .While when P is greater than Q then the comparator generates a high signal at that respective pin at the output. Similarly, when the magnitude of Q is greater than P then the output at pin showing P < Q will be high.

b) 2-BIT MAGNITUDE COMPARATOR:

For two inputs of 2-bit each, we will have 16 possible combinations. Therefore, in this case, the output will show high and low value depending on the comparison of the 2-bit value of binary input. Here we have provided the decimal equivalent of 2-bit binary values for both inputs P and Q in order to have simplicity in comparison . By observing the table, you can clearly check the different conditions for which the respective output is high. Like when both the inputs are same either 0 or 1 then the output pin representing P = Q will be high. Similarly, for all those conditions where the bit value of P is greater than Q, then the output pin representing P > Q will be only high . While when the magnitude of Q is greater than P then the respective pin representing P<Q will be high rest others will be low.

III.4-BIT MAGNITUDE COMPARATOR:

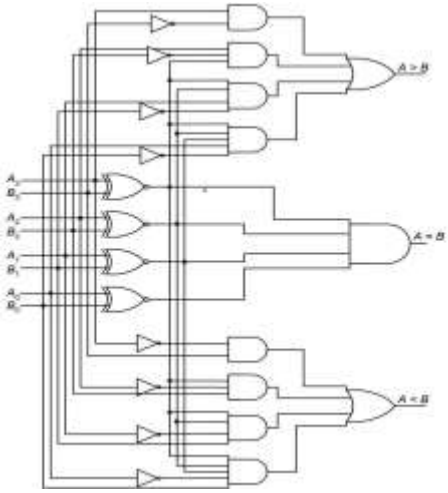

Figure 2 : 4-Bit Magnitude comparator using logic basic gates

A comparator used to compare two binary numbers each of four bits is called a 4-bit

magnitude comparator. It consists of eight inputs each for two four bit numbers and three outputs to generate less than, equal to and greater than between two binary numbers. In a 4-bit comparator the condition of A>B can be possible in the following four cases

1. If A3 = 1 and B3 = 0
2. If A3 = B3 and A2 = 1 and B2 = 0
3. If A3 = B3, A2 = B2 and A1 = 1 and B1 = 0
4. If A3 = B3, A2 = B2, A1 = B1 and A0 = 1 and B0 = 0.

Similarly the condition for A<B can be possible in the following four cases

1. If A3 = 0 and B3 = 1
2. If A3 = B3 and A2 = 0 and B2 = 1
3. If A3 = B3, A2 = B2 and A1 = 0 and B1 = 1
4. If A3 = B3, A2 = B2, A1 = B1 and A0 = 0 and B0 = 1

The condition of A=B is possible only when all the individual bits of one number exactly coincide with corresponding bits of another number.

INPUTS								OUTPUTS		
A3	A2	A1	A0	B3	B2	B1	B0	A > B	A = B	A < B
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	1	0	0	1
0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	1	0	1	0	0	1
0	0	0	0	0	1	1	0	0	0	1
0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	1	0	0	1	0	0	1
0	0	0	0	1	0	1	0	0	0	1
0	0	0	0	1	0	1	1	0	0	1
0	0	0	0	1	1	0	0	0	0	1
0	0	0	0	1	1	0	1	0	0	1
0	0	0	0	1	1	1	0	0	0	1
0	0	0	0	1	1	1	1	0	0	1
0	0	0	1	0	0	0	0	1	0	0
0	0	0	1	0	0	0	1	0	1	0
0	0	0	1	0	0	1	0	0	0	1
0	0	0	1	0	0	1	1	0	0	1

Figure 3: Truth table for 4-bit magnitude comparator

IV .Implementation:

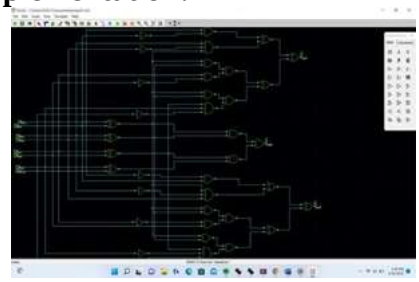

Fig 4 : 4-Bit magnitude compataror in DSCH

Fig 5 : Timing diagram for 4-Bit magnitude comparator

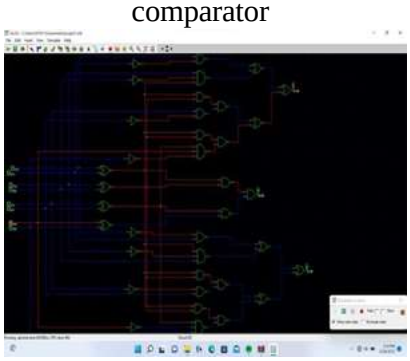

Fig 6: 4-Bit magnitude comparator for (A>B) condition

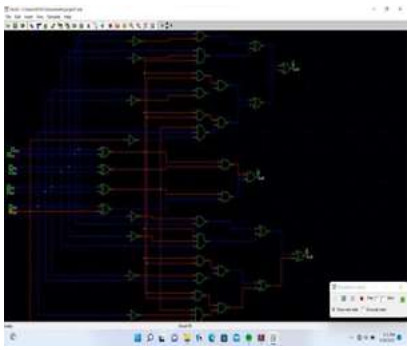

Fig 7 : 4-Bit magnitude comparator for (A<B) condition

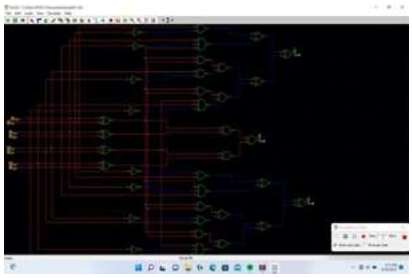

Fig 8 : 4-Bit magnitude comparator (A=B) condition

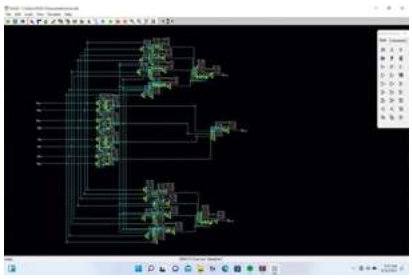

Fig 9 : CMOS 4-Bit comparator circuit in DSCH

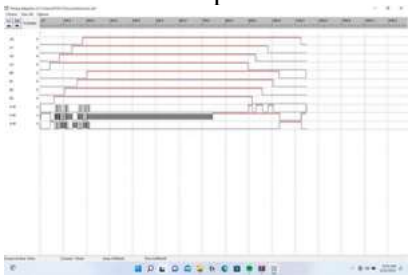

Fig 10 : Timing diagram for CMOS 4-Bit comparator

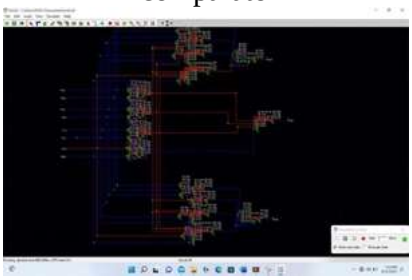

Fig 11 : CMOS 4-Bit comparator for (A>B) condition

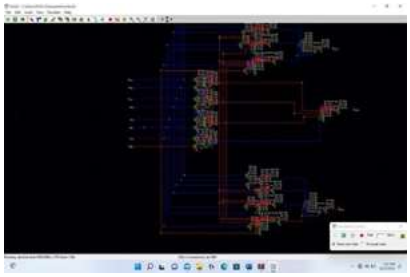

Fig 12 : CMOS 4-Bit comparator for (A<B) condition

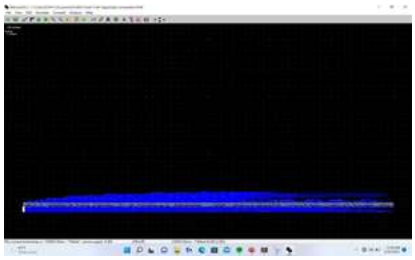

Fig 13 : CMOS layout design for 50nm technology node

Fig 14 : vdd at 1.2v for 50nm technology node

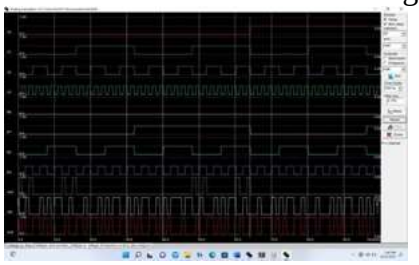

Fig 15 : vdd at 1.0v for 50nm technology node

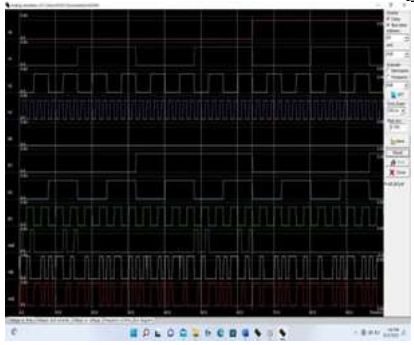

Fig 16 : vdd at 0.6v for 50nm technology node

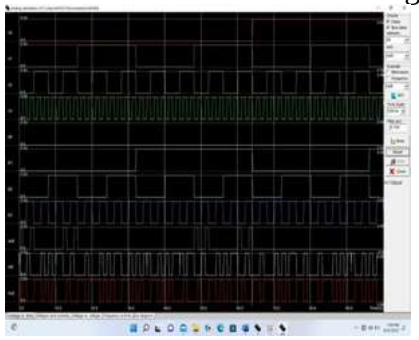

Fig 17 : vdd at 0.5v for 50nm technology node

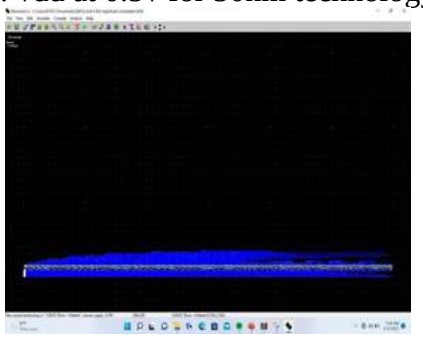

Fig 18 : CMOS layout design for 70nm technology node.

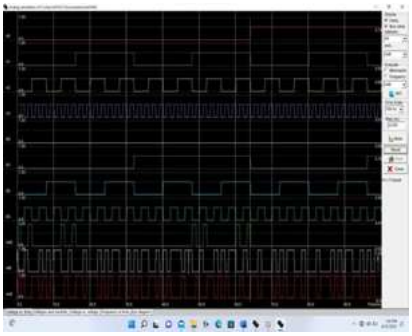

Fig 19. : vdd at 1.2v for 70nm technology node

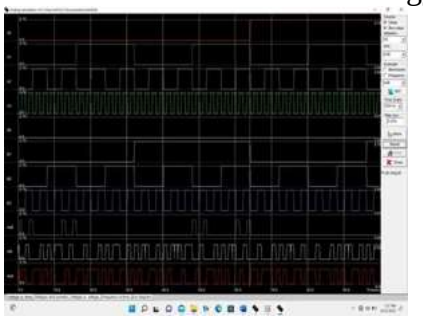

Fig 20 : vdd at 0.5v for 70nm technology node

Fig 21 : CMOS layout design for 90nm technology node

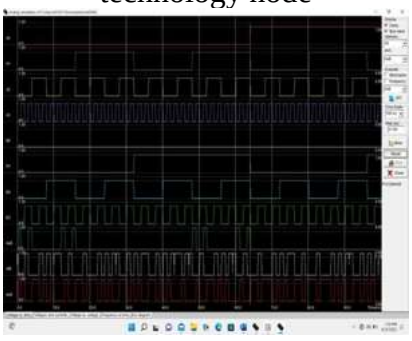

Fig 22 : vdd at 1.2v for 90nm technology node

50nm		70nm		90nm	
7 metal		6 metal		6 metal	
VDD	PD	VDD	PD	VDD	PD
1.2v	5.950mW	1.2v	1.719mW	1.2v	0.294mW
1.0v	1.339mW	1.0v	0.161mW	1.0v	97.555μW
0.6v	45.267μW	0.6v	24.916μW	0.6v	55.920μW
0.5v	7.526μW	0.5v	20.342μW	0.5v	31.529μW

Figure 23: Comparison

V. CONCLUSION:

In this project, we have deliberated the design procedures of a 4-bit comparator circuit in DSCH setting and then simulated the layouts at three different CMOS technology nodes of 50 nm, 70 nm, and 90 nm in Micro wind setting. Based on the performance comparison of various nodes, we have verified that the surface area occupied by the circuit increases as we increase the technology node 50 nm to 90 nm. Not only has that, the power dissipation and the propagation delay also increased with the increase of the technology node.

VI. FUTURE SCOPE:

In the future, more such performance parameter-based assessments may be done for the other digital logic circuits and systems. This type of simulation-based study is very much beneficial for the VLSI circuit design related theory and laboratory-based courses.

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