Recent Trends and Challenges onLow Power FinFET Devices

M. Chandra Sekhar Reddy[1], N. Yerriswami[2] , J. Hema Madhuri[3]
[1]Professor, [2]Assistant Professor, [3]Assistant Professor, ECE Department, Anantha Lakshmi Institute of Technology and Sciences, Ananthapuramu, Andhra Pradesh, India.

Abstract: Due to the rapid growth on electronic industries, the revolution on Integrated circuits still plays a major role. Over the last few years, research works on Integrated circuits is going on scale down the devices dimensions in order to attain small size as well as improvement in speed of circuits. Regardless of the progress in the area of VLSI design Bulk CMOS technology which consumes very less power. But one of the most important breakthroughs of this technology is short channeling property. In advanced digital application the key constraint is low off state leakage current, while we scale the device dimension. And it must maintain high driving capability. Here FinFET overcomes short channel effects as well as it exhibits high driving current capability even in nano scale channel. Recent developments in FinFET's have increased the need for off state leakage current along with high speed switching devices.

-In the past decade, a number of studies have sought to determine different FinFET based devices. Previous studies in this area of research have reported the types of FinFET's along with different applications. This paper presents a literature review on FinFET based different devices. And a bird eye review for advanced FinFET's is presented in this literature work. This literature work reviews on some research papers.

Keywords: Bulk CMOS devices, FinFET devices, short channel effects, off state leakage current power consumption.

1 Introduction

Over the past three decades, electronics revolution in an IC is scale down the devices dimensions from 320nm to 45nm. This scale down process is building blocks of CMOS technology. As the IC technology changes form micron devices to sub-micron devices, it has major factors like achieving low cost & high performance devices are the challenges for the production. But CMOS have its own constraints.

Many researchers will identify the drawbacks in cmos technology while we scale down the device dimension. Among those we have basic drawback of short channel effects will raise to bulk CMOS device OFF state transition leakage current. That bulk cmos devices doesn't meet the specifications of the industries, because of its lower transistor drive current. And gate oxide thickness is also an important issue while considering scaling factor. We have basic limitation for gate oxide thickness, when it crosses its limitation will cause an unexpected gate leakage current.

After this researchers will overcome those problems by making high permittivity gate dielectrics i.e. (High-K) [1]. When we maintain low sheet resistance will causes high driving current. Due to this reason technology gradually changes form bulk silicon CMOS devices to Ultra thin body transistors. This ultra thin body transistors leads to reduce sub surface leakage paths by making thin silicon on insulation process. But a thin body mos transistor consists of very high parasitic drain and source resistance. Figures of bulk type si mos transistor and ultra thin mos transistors are shown in below fig 1a and 1b. Ultra thin body mos transistors have least effective controlled gate.

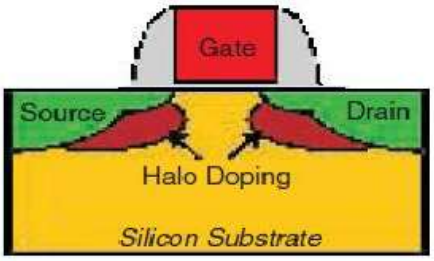


Fig 1.a Bulk mos transistor

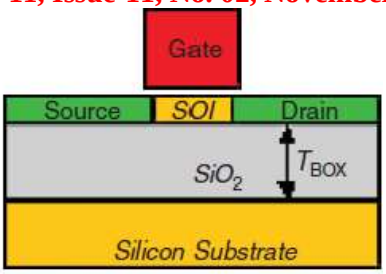


Fig 1.b Ultra thin mos device

For attaining high driving current through ultra thin body devices we have to maintain bottom silicon substrate body as thinner as we can. And thicker source and drain terminals will leads to minimizing the parasitic resistance. Hence these systems will drive high driving current. A new low pressure chemical vapor deposition process is included for thicker source and drain terminals. By increasing the threshold voltage of pmos transistor and nmos transistor of ultra thin body leads to decreases the thickness of the body. This body thickness has an impact on sub-band spacing. They both are inversely proportional to each other. This will leads to a decreasing the effective mass and increases the mobility factor. But the major challenges in ultra thin mos devices are having high series resistance of the thin body. This will overcomes by the FinFET devices.

In cmos we have lot of short channel effects with threshold voltage variations will overcomes by using the multi gate devices [1]. Multi gate devices are non planar devices. Which have in different modes like short gated mode, independent gated mode, and low power mode. Among those we considered short gated mode type multi gate transistors. These transistors have two gates which one gate is shorted to another gate for additional controlling to the gate terminal. Basic non planar FinFET devices shows in fig.2

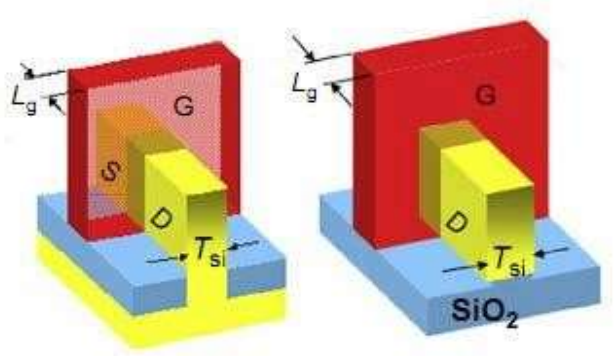


Figure.2 non-planar FinFET devices [2]

In this paper we present logic gates based realization of FinFET's. Basically we focused on Universal gates along with Xor and Xnor FinFET Design, through predictive technology model (PTM).

2 Trends in FinFET Logic Design

The literature on FinFET based Logic circuits shows a variety of approaches. Here we focused on most research papers regarding to FinFET devices. And also we verified those by using predictive technology and BSIM-CMG models. Circuit design parameters like Fin width, Fin height and Fin Pitch along with gate parameters are verified by using multigate MOSFET technology Springer article [2]

***A.* Massimo Alioto "Analysis and Evaluation of Layout Density of FinFET Logic Gates" 2009 IEEE International Conference on Microelectronics [3]**

In this paper author compared layout density between bulk CMOS logic gates and FinFET logic gates. Author considered FinFET 3T/4T logic gates .

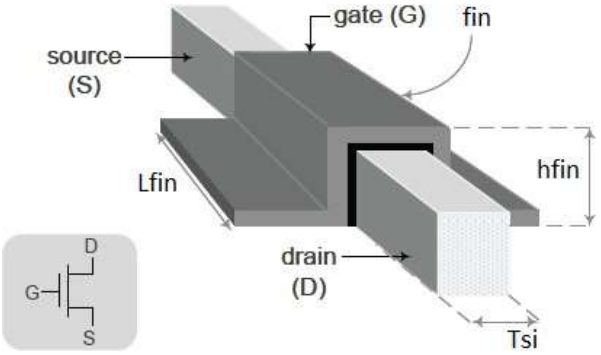


Figure 3(a). 3T FinFET physical structure [3]

Here author also mentioned the Area occupancy compared to the CMOS 65nm standard type to FinFET multigate transistor. This result shows that area overhead problem of planar CMOS bulky transistors overcomes by using n channel stacking process of FinFET devices.

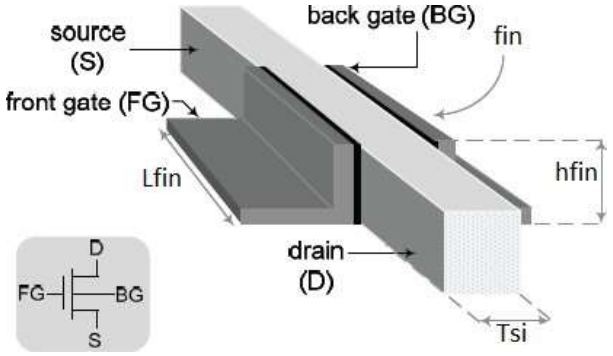


Figure 3(b). 3T FinFET physical structure [3]

B. **Ravindra Singh Kushwah, Manorama Chauhan "Modeling and simulation of FinFET circuits with Predictive technology models", 2014 [4]**

In this paper authors mentioned that basic four types of FinFET models i.e. SG mode (shorted gated mode), IG mode (independent gated mode), low power mode and hybrid IG-mode with LP mode (low power). Author consider one nand gate logic design through all FinFET models.

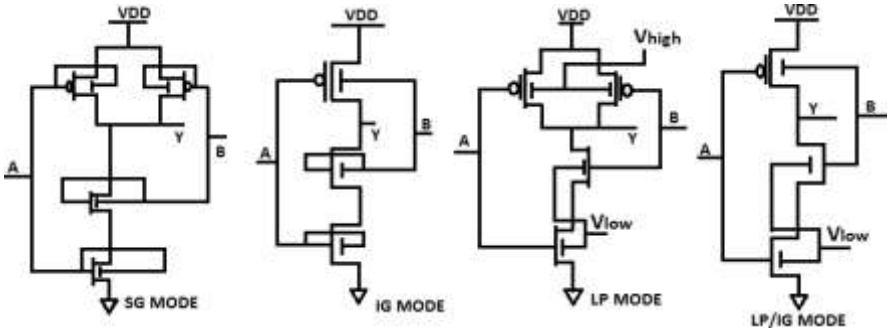


Figure 4. FinFET based NAND & NOR [4]

For simulation they are used BSIM-CMG 45nm technology with cadence virtuoso simulation tool. Author compared all the nand gate based models. Among those short gated model and independent gate model have high noise tolerance compared to low power gate and low powered independent gate model. And short gated mode and independent gate model have 40% of low leakage power, 25% of low power consumption and 20% of low tolerance compared to low power gated and low power independent gated model. Coming to the delay it is 10% of low power model and low power independent model compared to short gated model and independent

gated model[4]. And finally the speed, low power model has higher speed than the other models. Finally short gated model of FinFET nand gate design 35 to 45% of low leakage power than the other model FinFET nand gates. Independent gate and low power independent gate devices required very less no. of transistors means it occupies very less area compared to other models. But it has a design limitation like fin height and fin width.

C. Sapana S. Nalamwar, Prof. Smita A. Bhosale "Design of low power logic gates by using 32nm and 16nm FinFET technology" 2015 [5]

In this paper author verified that FinFET based nand and nor gates. Simulation is going through by using predictive technology model files of 32nm cmos and 32nm FinFET. Authors differentiate the factors of static power, dynamic power and current flowing through the cmos and FinFET systems using 32nm model and 16nm model.

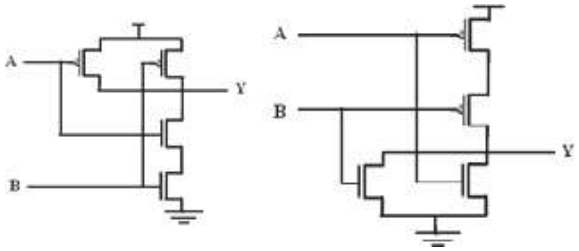


Figure 5. FinFET based nand & nor [5]

And they applied According to the results 0.8v is the minimum to operate the cmos and FinFET device at 32nm model. And for 16nm model cmos doesn't operates. But in case of FinFET it will operates at 0.3v. The dynamic power issue in FinFET nand gate it is 436.61 nW, for nor gate it is 439.99 nW in 32nm model [5]. Where in 16nm model it is reduced to 187.30nW for nand and 200nW for nor gate. Hence author said that when we decreasing the channel length of the device in FinFET then it will greatly reduces dynamic and static power of the device. And also compared to nor gate based FinFET, nand gate based FinFET device have better static and dynamic power consumption.

D. Cristina Meinhardt and Ricardo Reis "FinFET Basic Cells Evaluation for Regular Layouts", 2013 IEEE [7]

In this paper author designed independent gate based FinFET Nand gate design and observed it significantly improved delay and power factors of the previous cases. Independent gate FinFETs achieved area reduction up to 20% compared to the other low power FinFET gate models [7].

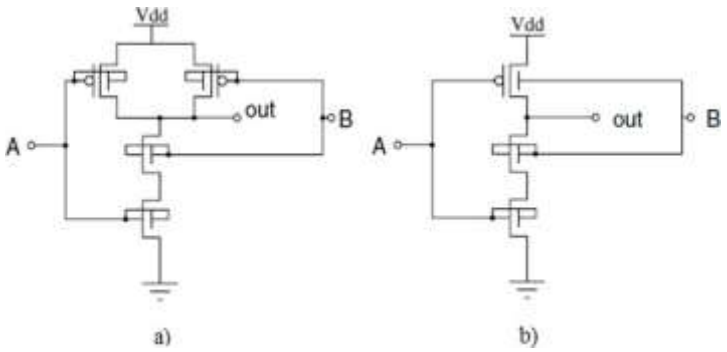


Fig 8. FinFET based SG-mode NAND & NAND [7]

Author compared all three designing models of FinFET and observed power, timing and area constraints of the nand gate design. Independent gate FinFET are similar to CMOS bulky transistor but the operation of transistor is slower than the Short gated FinFET devices. In power parameter independent gate FinFET mode consumes very less power. but it has its own limitations.

E. Cristina Meinhardt, Ricardo Reis "Comparing High-Performance Cells in CMOS Bulk and FinFET Technologies", 2014 IEEE [8]

This paper is an extension of pervious case of regular layout design process.

But in this paper author verified 32nm technology library.and results are compared with static and dynamic power dissipation of the device.

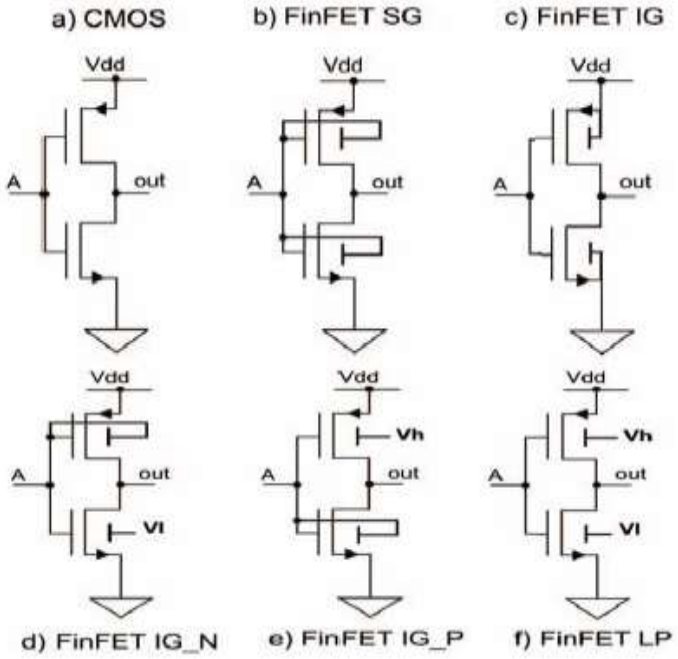


Fig 8.CMOS & FinFET SG, IG, and LP mode [8]

By using the predictive technology model PTM of FinFET gives you better delay result compared to TCAD simulation tool. But it has extensively increasing the design rules based layout design [8]. Regular layouts may have an effect of routing problems

F. Xuqiang Zhang, Jianping Hu, Xiaoyan Luo "Optimization of Dual-Threshold Independent-Gate FinFETs for Compact Low Power Logic Circuits", 2016 IEEE [9]

In this paper author designed independent gate FinFET design compared to short gated FinFET model.

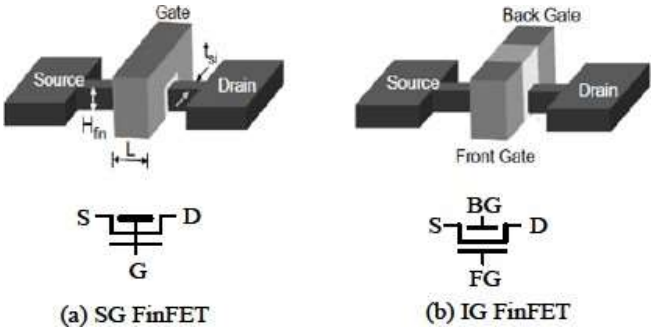
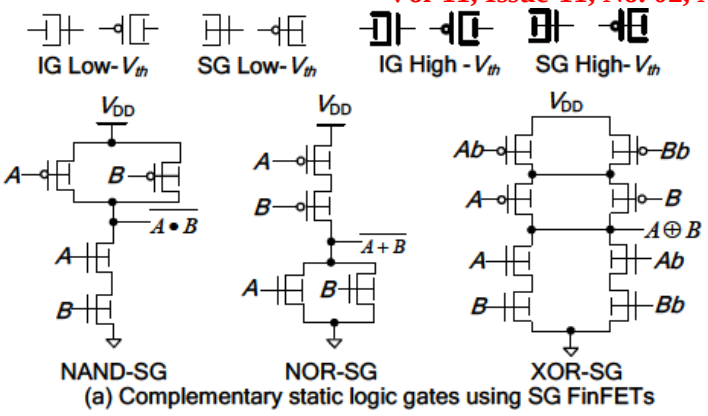


Fig 9. FinFET based SG-mode & IG- NAND [9]

Author designed independent gate mode and short gated mode FinFET NAND and NOR circuits along with differential cascade voltage switching logic based xor and xnor circuits.



(a) Complementary static logic gates using SG FinFETs

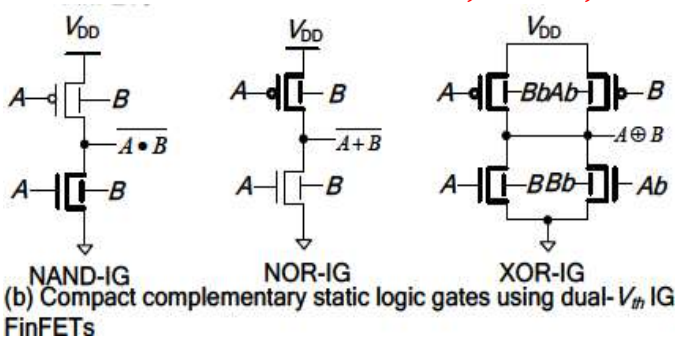


Fig 10. FinFET based SG,IG-mode NAND, NOR & XOR [9]

The result of short gated mode is compared with dual threshold independent gate FinFET mode device. By using dual threshold IG mode FinFET based static and DCVSL[9] will get low power delay compared with Short Gated FinFET's.

G. Neha Yadav, Saurabh Khandelwal, Shyam Akashe "Design and Analysis of FINFET Pass Transistor Based XOR and XNOR Circuits at 45 nm Technology",2013 [10]

In this paper author designed xor and xnor system based on FinFET pass transistors logic. And also along with this they considered short gated model for designing xor and xnor systems.

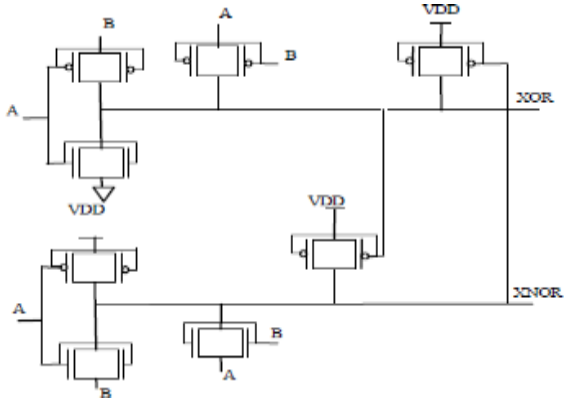


Fig 12. FinFET based IG-mode XOR-XNOR mode [10]

Author verified product of power delay and energy delay for xor and xnor FinFET devices consumes very less power and high speed systems compared to other models in FinFET's. But it has certain limitations to design below 45nm[10].

H. Sarada Musala, Student Member, IEEE, Avireni Srinivasulu, Senior Member, IEEE "FinFET Based 4-BIT Input XOR/XNOR Logic Circuit", 2016 IEEE [11]

In this paper Author designed 4 bit XOR/XNOR circuit using pass transistor FinFET logic. With a full voltage swing at the output will produces good driving capability at high frequencies also.

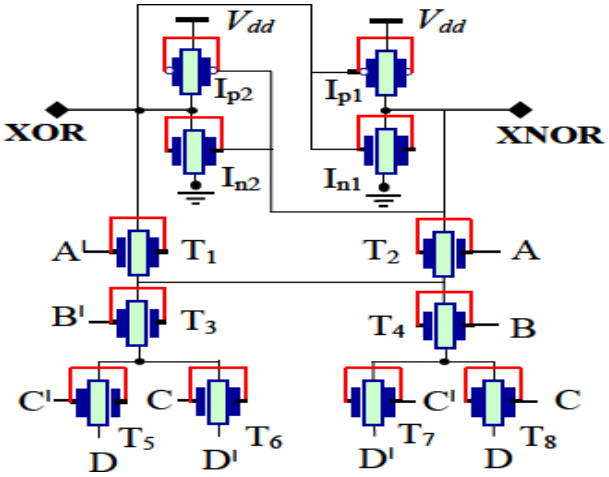


Fig 13. FinFET based XOR-XNOR [11]

The structure is simple to design. This pass transistor based FinFET design has very less delay because of its critical path consists of less number of transistors. And also author verified power consumption is also better than previous case.

3 Challenges in FinFET based Design

An advanced FinFET device has multi-gate short circuit gate mode and independent gate mode 3D transistor. While compared to CMOS bulky planar transistors, FinFET has efficient improvement in power consumption and performance. And also it has better electrical property along with great reduction in dynamic power as well as static (leakage) power.

For an advanced FinFET technology i.e. 10nm technology, it has some major design challenges. These are in analog, digital, parasitic and signoff perspectives..

- While fabricating the FinFET device we need an additional masking for correct printing at below 20nm design technology
- For layout designing at 28nm or below becomes more complicated with additional nodes requirement.
- For the metal layers resistivity it consists of 50 Times or more potentials are required
- For all the low process node operation Electro-migration will dramatically increases
- More number of complicated fabrication based design rules
- As we design millions of gates in fabrication gives an more time to market

But it had an advantage for Designers can improved performance by working at lower voltages.

4 Conclusion

In this paper presents a review on FinFET based logic gates. FinFET devices are advanced devices which greatly reduces our short channel effects in cmos devices. As well as when we scale down the channel length of the device static and dynamic power is also reduced. We considered design parameters of FinFET devices and also how those FinFET parameters are modeled by using Predictive technology model. Various FinFET models also discussed in this review papers.

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