DESIGN OF AN AREA-EFFICIENT AND LOW POWER 32 BIT SAR ADC FOR BIOMEDICAL APPLICATIONS.

G.Vijaya Deepthi, PG Scholar, Department of Electronics and Communication Engineering, CMR Institute of Technology, Hyderabad, Telangana,(Affiliated to JNTU Hyderabad and Accredited by NBA New Delhi)
Dr. K. Niranjan Reddy, Professor &HOD, Department of Electronics and Communication Engineering, CMR Institute of Technology, Hyderabad, Telangana, (Affiliated to JNTU Hyderabad and Accredited by NBA New Delhi)

Abstract
This project provides a low-power consumption 32-bit SAR ADC. In recent years, In medical applications such as pacemakers, the need for Successive Approximation Register (SAR) Analog-to-Digital Converters has skyrocketed. The need for extended battery life in these applications necessitates the development of low power SAR ADCs. To improve conversion speed, SAR ADC employs a comparator. Furthermore, the CMOS sample and hold circuit is intended to compensate for charge injection. The SAR logic has been enhanced, as has the conversion speed. This design employs R-2R DAC. R-2R DACs are favored among all DAC designs because to their decreased design complexity. To boost accuracy, The R-2R ladder network was used to construct DAC subblocks in order to increase conversion speed and reduce power consumption. As technology advances, digital solutions will give improved mobility and flexibility across IC manufacturing processes, resulting in reduced power and cost. The efficacy of the suggested SAR ADC has been shown by simulation results. The ADC will be constructed in 45nm CMOS using the CADENCE virtuoso tool.
Keywords: Analog-digital converters (ADC), data conversion, low power, successive approximation register architecture (SAR), digital to analog converter (DAC).

Introduction

The world of wireless transceiver demands faster and more energy efficient ADC for various future application, such as 5G wireless communication standards, and industrial control system. Among all the ADC architectures, SAR ADCs are especially known for its extreme low power, and are mostly designed and utilized in low frequency and ultra-low power applications, such as medical instruments. SAR ADCs are especially well-suited for hybrid systems that test the limitations of other kinds of converters, such as pipeline or oversampled ADCs, in addition to being an outstanding option as a stand-alone or time-interleaved design. Highly effective integration ADCs are crucial to digital processing because they are the interface circuits that link the analogue and digital worlds. SAR (Successive Approximation Register) ADCs have been more popular in recent years gained favor because to their low power consumption and digital friendliness. Due to the binary search approach, Although SAR ADCs have a high conversion rate, slower than other ADC designs. This paper describes a 32-bit SAR ADC that uses a comparator to improve conversion speed. Furthermore, the CMOS sample and hold circuit is intended to compensate for charge injection. The SAR logic has been enhanced, as has the conversion speed. R-2R DAC is employed in this design since it is the most common DAC architecture. Because of their decreased design complexity, optimum power, and enhanced matching, R-2R DACs are chosen. As technology advances, digital solutions will give improved mobility and flexibility across IC manufacturing processes, resulting in reduced power and cost. The efficacy of the suggested SAR ADC has been shown by simulation results. The suggested design employs 45nm CMOS technology. Pacemakers have direct control over the pulse rhythm and pace. When the heart stops or beats too slowly, the pacemaker sends out weak electrical impulses at 70 beats per minute to correct the timing of the heartbeat. This medical equipment is equipped with a battery, a generator, and pacing lines. The leads link the pacemaker to the heart and stimulate it with the pacemaker's pulses. The battery and generator are housed in a

titanium container within the body.

The artificial pacemakers' lifespan should be up to ten years, with minimal power consumption each operation. The analogue-to-digital converter is a crucial component of an implanted pacemaker because It serves as a bridge between the digital signal processing block and the analogue signal that was detected. As a result, lowering the ADC's power consumption is a crucial problem. The analogue-to-digital converter is a crucial component of an implanted pacemaker because it acts as the interface between the detected analogue signal and the digital signal processing block. Because of its simplistic design, it uses less electricity. Furthermore, since most of the design is digital except for the comparator, SAR ADC is scalable with technology scaling.

Review of Literature

This research built a 1.2V 8-bit SAR ADC. Cadence Virtuoso was used to implement the schematic diagram of several subblocks utilizing 45nm technology. The comparator was developed using a differential amplifier to remain in saturation. We focused on the power-hungry comparator. The DAC subblock's R-2R ladder network improves precision. The ADC was driven by asynchronous control logic written in Verilog, eliminating the requirement for a clock [1].

This work presents a single-channel asynchronous SAR ADC with dual trail switching mechanism. While the comparator is being generated, the proposed design employs two capacitive DAC arrays to provide two potential outputs. Each DAC is allocated two comparators that alternate between the compare and reset phases. This approach overlaps DAC settling, comparator reset, and comparator regeneration, improving conversion performance. Mismatches between channels are turned into wideband noise, which improves SFDR[2].

A wideband multi-standard asynchronous SAR ADC is presented in this work. There are three ADC settings that may be used: 80 MS/s 10-b, 40 MS/s 11-b, and 20 MS/s 32-b. The bandwidth of time-interleaved sampling is increased, but the resolution is reduced.

The digital calibrating procedure cancels out channel incompatibilities. The sampling switch employs Bulk-biasing reduces top-plate charge injection. Asynchronous processing increases speed/resolution tradeoff flexibility. Switching energy is reduced by using a two-step digital-to analog converter (DAC). Using 2.61/2.05/1.77 mW of power, the 45-nm CMOS ADC achieves an SNDR of 56.7/61.2/64.6 dB and an SFDR of 72.3/74.8/75.5 dB at sampling frequencies of 80/40/20 MHz[3].

In this work, two switching approaches are used to examine the linearity of SAR ADCs with split DAC structures. Standard charger distribution and Vcm switching The static linearity performance of the split DAC is assessed here, including integral and differential nonlinearity. The traditional SARADC's conversion nonlinearity may be corrected using a code-randomized calibration technique which is confirmed by simulations and data. In 90 nm CMOS, the performance of both switching approaches is proven. The advantages of Vcm-based switching may be readily shown in terms of power, speed, and linearity measurements[4].

Analog-to-digital converters (ADCs) are the subject of this research for data collection employing a completely CMOS high speed self-biased comparator circuit. When space and performance optimization are important, ASICs are in great demand, and their 45nm designs are optimized in CADENCE virtuoso. Tower jazz semiconductor foundry supports layout design and GDSII extraction. The design technique compares many DAC designs to find the one with the lowest DNL and INL. This article describes the design of a 9-bit SAR ADC with a 0 to 2.5V input voltage range and 16.67 KHz sampling frequency. For the simulations, H spice simulators are employed [5].

DAC capacitor swapping in a SAR ADC has never been done this way before. The average switching energy of the array may be decreased by 37% by separating the MSB capacitor into binary scaled sub-capacitors. A 10b capacitor array HSPICE simulation on a 0.18m CMOS process backs up the equations[6].

This paper designs and models an 8-bit SAR analogue-to-digital converter using TSMC 0.18-m

CMOS. A DAC with two attenuation capacitors is employed in this ADC to reduce power consumption and DAC settling time. In addition, Dynamically biased comparators reduce power consumption. When the input voltage difference is high. There is no need for a large bias current. The CS stage recognizes the common node of the differential input pair and increases Mbias' VT to identify a big input difference[7].

A rapid, analogue implementation of the DFT/ lDFT necessitates answers to the I/O bottleneck experienced by huge, parallel input sequences, the sluggish execution time of lengthy sequential sequences, and the resulting error. We offer an architecture that balances input serialization, circuit area, execution time, and output error using multiple changes to Goertzen's Algorithm[8].

This research presents a bio impedance measuring tool with a wide range of configuration options for use in a variety of healthcare settings. A high-resolution ADC and digital processing replaces complex, space-consuming analogue components. designers and users more flexibility. The 0.18m CMOS prototype system architecture is proposed. The signal generator's tuning range is 10kHz-10MHz, and the VCCS fluctuates less than 1%. Gain, bandwidth, CMRR, and input referred noise are 18dB, 1.5Hz to9.5MHz, and 96.7dB at 100kHz. ADC uses a pseudo differential VCO. ADC has SNR, SFDR, and SNDR of 87.5dB, 60dB, and 60dB, respectively. The prototype uses 6.7mW[9].

COMPARATOR:

A comparator is a circuit that compares two inputs and generates an output If the comparator's output is greater than zero, it indicates that the input is more than zero. The comparator is a non-linear IC application, so keep that in mind. An op-amp consists of two terminalsandiscomparedbyanbasedcompartorCompares the two inputs applied to it and produces the correspondingresult as theoutputThis portion discusses comparators based on op-amp.

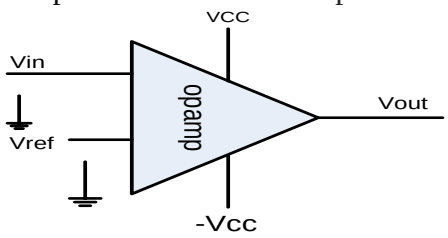


Figure 1: Comparator Circuit

Working

In most cases, a specialized voltage comparator will be faster than an operational amplifier. A dedicated voltage comparator may also have Internal voltage reference, configurable hysteresis, and a clock-gated input are all included in this device. This is a voltage comparator that is especially intended for use with the digital logic interface. A binary state is typically utilized to connect the physical world to a digital circuit.

For instance, if a fixed voltage source is in the signal path from a DC- adjustable device, a comparator is equal to the amplifier cascade. If the output voltages are almost identical, Analogue signals will enter the digital domain because the output voltage does not meet one of the logic levels. The amplifier cascade's gain is powerful so that this range may be narrowed as much as possible.

The comparator circuit shown in the figure above does not use feedback. Between Vin and Vref, the circuit amplifies, creating Vout. If Vin exceeds VREF, the Vout voltage will result in an increased saturation rate. i.e. favorable side voltage. If Vin is smaller than Vref, it will drop to its adverse side, i.e., adverse side voltage. Practically this circuit can be integrated to decrease noise with a range of hysteresis voltage. Even when the Vin signal is loud, the above circuit will provide stable operation.

There are several disadvantages in the practical use of use an operational amplifier instead of a specialized comparator-amps are intended to work with negative feedback in linear mode, so it has a saturation retrieval time. Nearly all op-amps have inner compensation capacitors for high frequency signals that impose slew rate constraints. A comparator is intended to generate output voltages that

are well-constrained and readily interfaced with digital circuitry. Using an operational amplifier as a comparator, digital logic compatibility should be examined. When employed as comparators, certain multi-section op-amps may exhibit some channel-to-channel communication. Many operational amplifiers feature diodes between their inputs. The inputs of the op-amps follow each other, but the comparator does not. The diode may cause an unexpected current to flow through the inputs.

SAMPLE AND HOLD

A sample and hold device samples the voltage of a signal that fluctuates continuously and maintains its value at a constant level for a predetermined period of time. Peak detectors, which are basic analogue memory devices, are connected to sample and hold. These are used in analog-to-digital converters to reduce fluctuations in the input signal that might interfere with the conversion process.

Samplingtime: The time the input signal sample is generated is called the sampling time (usually 1us to14us).

Holdingtime: When the switch is opened, i.e. when the pulse is ON, the time duration of the circuit t o hold the sampled value is called holding time.cap charges to its peak value.

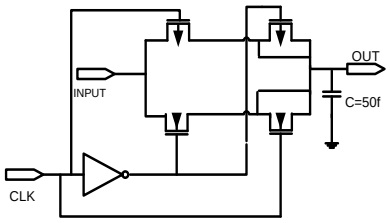


Figure2 :Sample and Hold Circuit

Digital to Analog Convertor (DAC)

The digital converter is the device that transforms digital data to analogue data. Based on this switch situation (ON / OFF) and position (MSB or LSB), the output analog amplitude is calculated using the digital data in the form of 1s and 0s used to control the switches in an analogue circuit with reference voltage.

R-2R DAC:

The R-2R DAC is a variant of the binary weighted resistor ladder DAC type that employs just two resistor values resistors may be connected in series with the value of R, and the 2R rung can be represented in current or voltage mode depending on the voltage reference. When operating in voltage mode, the ladder resistor is connected to Vref, and when operating in current mode, the output is connected to ground. R-2R DAC has the advantage of requiring just resistors with two resistance values, where 2N is the number of resistors. Because each rung of the ladder has a constant 2R resistance, this model's output impedance is always constant. In combination with the resistor ladder network, to improve the system's linearity, current source transistors are used. Adjusting the reference voltage between ground and digital level requires the use of a physical amplifier. The usage of the op amp output buffer restricts the bandwidth and might cause linearity issues.

Successive approximation A/D converter

1.A sample-and-hold circuit that measures the input voltage (Vin)

2.A comparator compares Vin with the DAC's internal output and outputs.

3. A successive approximation register subcircuit is intended to provide an internal DAC with a digital code of Vin.

4. An internal reference DAC provides an analogue voltage equal to the output of SAR in to the comparator for comparison with VREF.

The DAC and comparator settling time, which must resolve a minor variation in input voltage within the prescribed time, are the primary constraints on the SAR ADC's speed. The resistive construction

of the ladder is used by the DAC.SAR-ADC is an architecture that allows you to choose applications with medium-high resolution and slow-to-medium sampling rates. The maximum sampling rate for SAR is 5 mega samples per second (MS/S). Resolution of SAR ADCs will range from 8bits to 32bits and ADC provides small die area along with low power consumption. By this combination, these converters are ideal for large uses such as portable devices and data/signal acquisition.

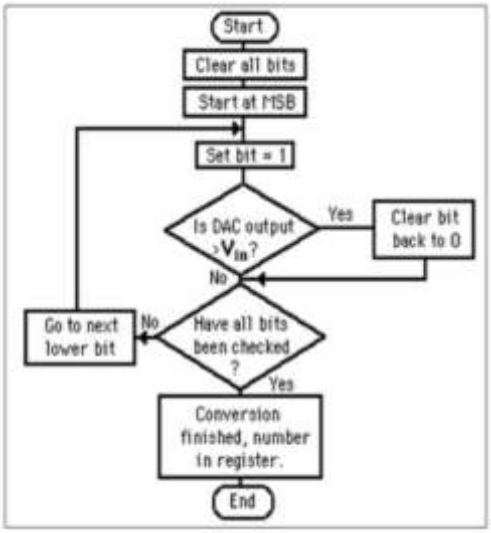


Figure 3: Flow chart for SAR ADC

The Binary Search algorithm is used in this. Internal circuitry will be significantly quicker than the total ADC sampling rate. A value is assigned to the successive approximation register such that the most significant bit equals 1. This code is delivered to the DAC, which compares the voltage sampled input using digital code (Vref/2) in the comparator circuit. If the analogue voltage exceeds Vin, the comparator may reset or keep the bit unchanged. The next bit will be set to 1 and the same test will be done until each bit in the SAR has been examined. The final output of the SAR will be in digital sampled input approximation at the conclusion of the EOC translation. The bulk of the market for ADCs with medium to high resolution consists of successive approximation register (SAR) devices (ADC).

Low power consumption, good precision, and a reduced device area are all advantages of SAR ADC. As a result of these advantages, the ADC is appropriate for a wide range of applications, including battery-powered portable equipment. Sensors and their electronics usually operate at medium speeds varying from a few kHz to a few MHz in the agricultural surveillance scheme.

To convert the analogue signal to digital signal, an ADC is required for post-processing purposes. The need for a low-power device makes a appropriate candidate for SAR ADC. This document produces a single-ended 10-bit SAR ADC based on the CMOS method the DAC is the SAR most critical element and it's hard to design. The DAC and comparator settling time, which must resolve a minor variation in input voltage within the prescribed time, are the primary constraints on the SAR ADC's speed. The resistive construction of the ladder is used by the DAC.

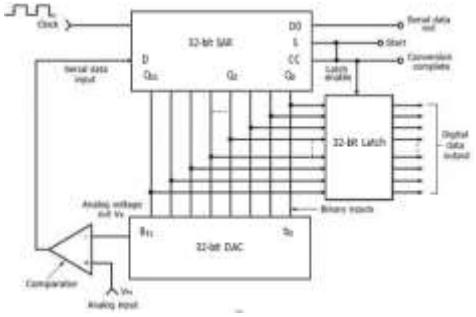


Figure 4: Block Diagram of SAR ADC

Low Power Technique:

VTCMOS Technique (Body Biasing)

In CMOS logic circuits, using low supply voltage (VDD) and low threshold voltage (VT) is an effective means of minimizing total power consumption while retaining high speed output. When performance is not available, constructing a CMOS logic gate using low-VT transistors would result in greater sub-threshold leakage and hence higher stand-by power consumption. One solution is to alter the transistor threshold voltages to prevent leaking. in standby mode, by changing the bias of the substratum.

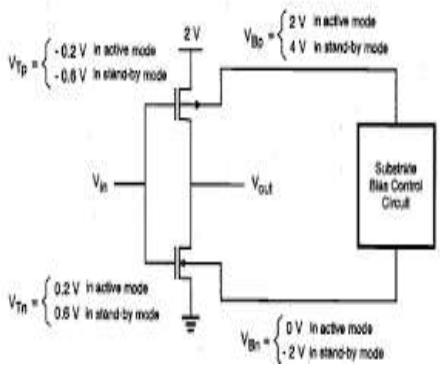


Figure 5: VTCMOS circuit

In conventional CMOS logic circuits, the substratum terminals of all NMOS transistors are connected to ground, while all PMOS transistor substratum terminals are connected to VDD. On the other hand, As shown in Figure, the substratum The variable substratum bias control circuit generates the bias voltages for nMOS and pMOS transistors in the VTCMOS circuit technology. VOn=0 is the substratum bias voltage for the NMOS transistor and the PMOS transistor's substratum bias voltage is VBP= VDD. As a result, there is no reverse gate-bias effect in inverter transistors. The circuit runs with a higher VDD and a low VT, resulting in less power dissipation (as a consequence of the low VDD) and rapid switching speed (due to low VT).When the inverter circuit is idle, the substratum bias controller lowers the NMOS transistor's bias voltage and raises the PMOS transistor's bias voltage. Consequently, threshold voltage magnitudes Due to the influence of the back gate's bias, VTl and VT both rise in stand-by mode. Since the present subthreshold cutoff. With this approach, Increasing the threshold voltage may significantly reduce the leakage power dissipation in standby mode exponentially.

RESULTS

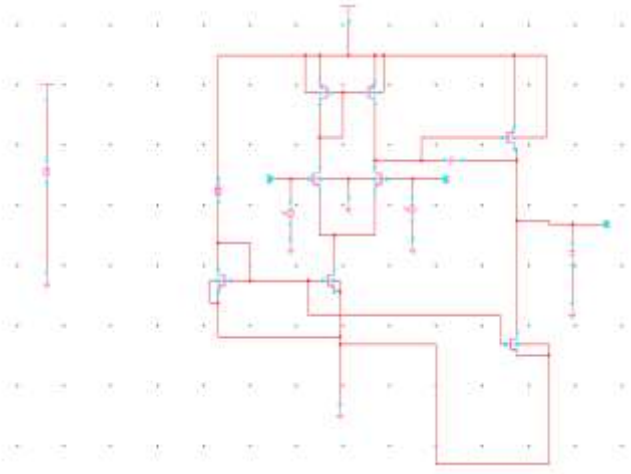


Figure 6: Schematic of operational amplifier

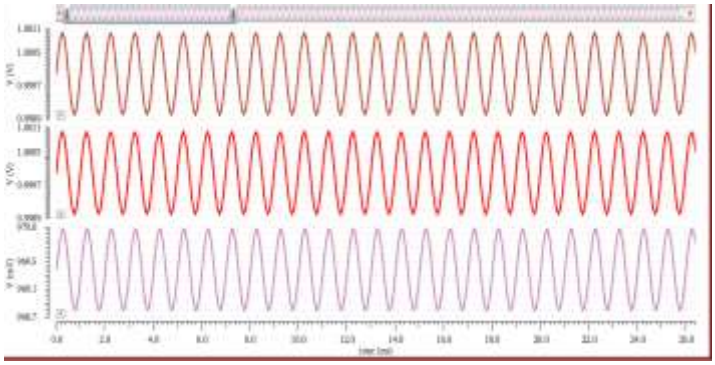
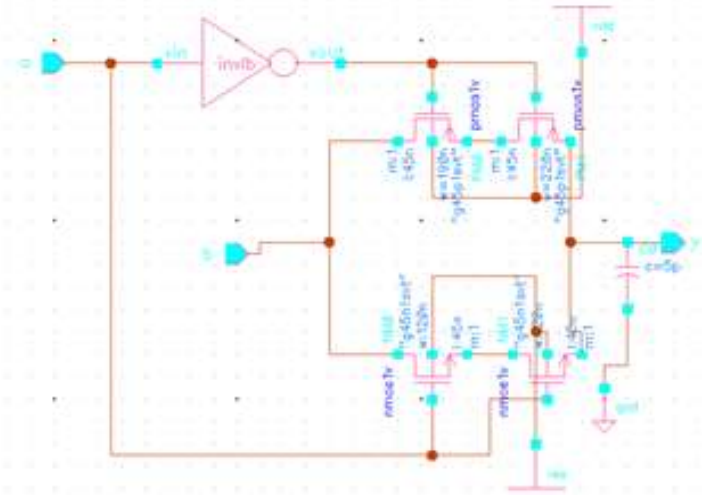


Figure 7: Simulation results of operational amplifier



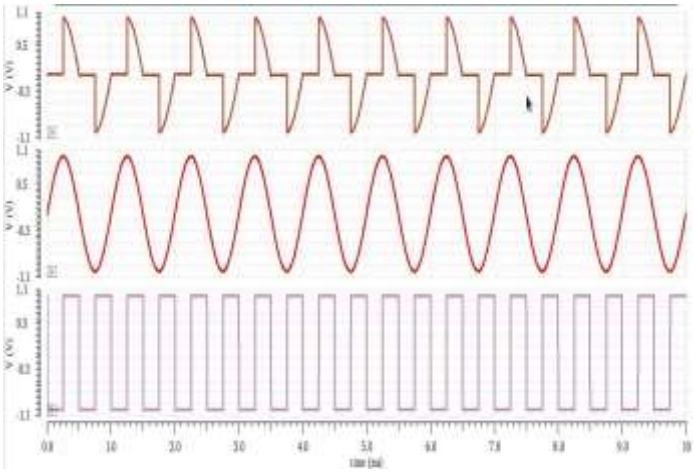


Figure 8 : Schematic of Sample and hold circuit
Figure 9:Simulation results of sample and hold

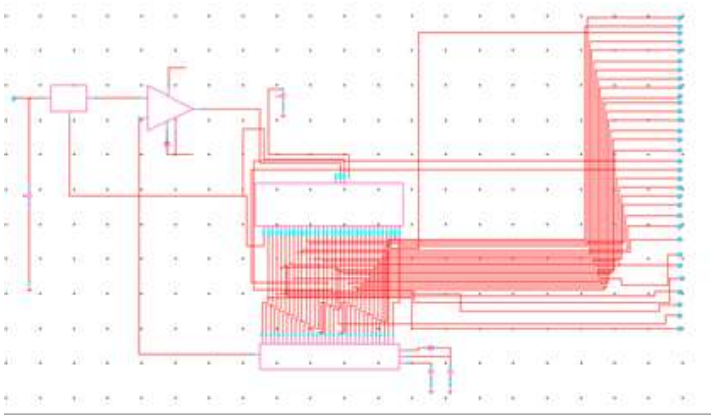


Figure10: Schematic of overall 32bit SAR ADC

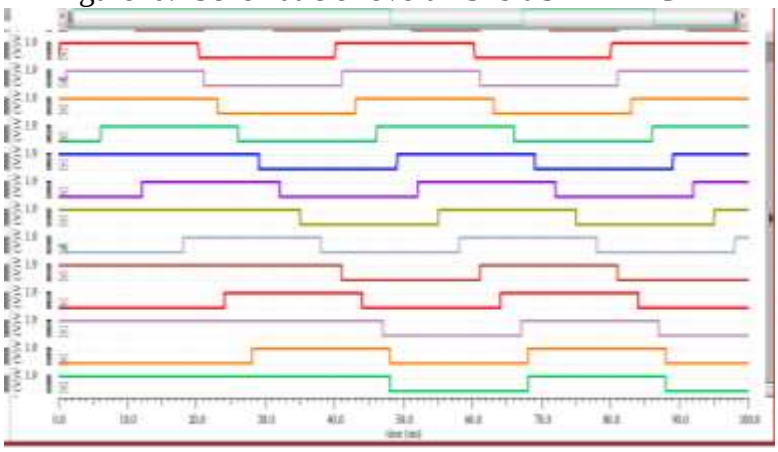


Figure11: Simulation results of 32- bit SAR ADC

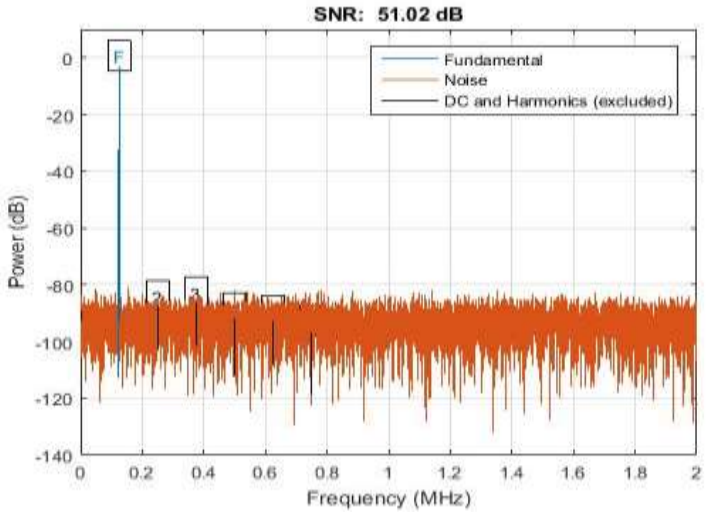


Figure12: SNR

	This work	[7]	[8]	[6]	[9]
Architecture	SAR	SAR	SAR	SAR	SAR
VDD[V]	0.8	1	1	1	1.2
Power	588.8 µW	127.8 µW	820µW	0.98 mW	0.826 mW
Technology(nm)	45	180	65	90	130
Resolution (bits)	32	10	10	10	10
DNL(LSB)	+0.66/-0.52	-	-	-	+0.91/-0.63
INL(LSB)	+0.4/-0.33	-	-	-	+1.27/-1.36
SFDR (dB)	63.97	-	75.2	-	65.9
SNR (dB)	51.02	-	56.9	57	57

Table 1 : Performance Comparison

CONCLUSION

The ADC should use as little power as feasible and take up as little space as possible while retaining correct, precise functioning over the whole spectrum of operation. As a result, the SAR control logic's power consumption is greatly lowered. Using SAR logic, they are constructed and compared in terms of power consumption and speed. Comparator design is a vital aspect of ADC development. The R-2R ladder network was utilized to create the DAC subblock in order to boost accuracy. To increase conversion speed and reduce power consumption. SAR ADC has grown in importance as a study area It is used in applications that need medium resolution, quick speed, low power consumption, and a tiny footprint. It is now a viable option for biological applications as well. With the exception of the comparator, save for the comparator, the vast majority of its blocks and components are digital, reducing its power consumption and allowing for technological expansion. To maintain the transistor in the saturation area, a common source amplifier stage was utilized as a second level of amplification.

REFERENCES

1. Ayash Ashrafi, Shania Ashram, Navaid ZafarRizvi, Shakeel Ahmad Dar " Low power Asynchronous SAR ADC",2016.
2. Lin He, Member, IEEE, Jaiqi Yang, DuonaLuo, Lele Jin, Shuangshuang Zhang, Fujiang Lin, Senior Member, IEEE, Libin Yao, Senior Member, IEEE, Xicheng Jiang, Fellow,IEEE "A Speed Enhancing Dual Instantaneous Switching Architecture for SAR ADCs",2013.
3. Yi Shen, Zhangming Zhu, Shubin Liu, and Yintang Yang "A Reconfigurable 10-to-12-b 80-to-20-MS/s Bandwidth Scalable SAR ADC",2017.
4. Yan Zhu, chi-Hang Chan,U-fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins, and Franco Maloberti "Split-SAR ADCs:Improved Linearity With Power and Speed Optimization",2013.
5. AKHIL, SUNIL JACOB M.Tech Student, Associate Professor, ECE department, SCMS School of Engineering and Technology, Kochi, Kerala, India "Design of 9 BIT SAR ADC Using High Speed and High Resolution Open Loop CMOS Comparator In 180NM Technology With R-2R DAC Topology",2014.
6. Brain P.Ginsburg and Anantha P. Chandrakasan Department of Electrical Engineering and Computer Science Massachusetts Institute of Technology, Cambridge, MA 02139,

USA "An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC",
7. Asadollah Salimi Department of Electrical Engineering, Boroujen Branch, Islamic Azad University, Boroujen, Iran "Design and Simulation of an 8-Bit Succesiive Approximation Analog to Digital Converter",2012.
8. Bing-Fei Wu and Chung-Fu Lin "Performance of a Fast Analog VLSI Implementation of the DFT",[1992] Proceedings of the 35th Midwest Symposium on Circuits and Systems,pp-1353-1356, 12 August 1992.
9. M.C. Cho, Y.G. Yoon, S.H. Cho, "Design of highly Programmable bio- impedance measurement IC in 0.18µm CMOS, "Intl. Soc Design Conference (ISOCC), pp. 79-82, Nov.2009.
10. Terence C. Randall, Ifana Mahbub, Syed K. Islam "Reconfigurable Analog-to-Digital Converter for Implantable Bioimpedance Monitoring"2015 IEEE Topical Conference on Biomedical Wireless Technologies, Networks, and Sensing Systems (Bio wireless),pp.32-34,2015.
11. B. Buchanan *,V. Madisetti **, M. Brooke * "A Rescheduling and Fast Pipeline VLSI Architecture Lifting- based Discrete Wavelet Transform",Proceedings of the 2003 International Symposium on Circuits and Systems,2003. ISCAS '03,pp-732-735.
12. Richa Dubey, Anjan Kumar, Manisha Pattanaik, "Design of Low Noise Low Power Two Stage CMOS Operational Amplifier Using Equivalent Transitor Replacement Technique for Health Monitoring Applications" .Fifth International Conference on Computing, Communications and Networking Technologies (ICCCNT),11-13 july 2014.
13. TriptiKachar, ShrutiSuman, p. K. Ghosh3, "Design of High Gain Low Power Operational Amplifier"2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICCEOT),PP.2370-3274,24 November 2016.
14. Mohsen Mohammadpour*,MasoudRostampour, "Indirect Miller Effect Based Compensation in Low Power Two-Stage Operational Amplifiers",2012.
15. B.Murmann.ADCPerformSurvey1997[Online].Available:http://www.stanford.edu/~murmann/adcsurvey.html.2014
16. Axim integrated nc. "understanding AR ADCs: Their Architecture and Comparison with Other ADCs:"Maxim Tutorial 1080, 2001.
17. E. Alpman, H. Lakdawala, L.R. Carley, K. Soumyanath, " A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP digital CMOS, " Solid-State Circuits Conference - Digest of Technical Papers (ISSCC), IEEE International, pp.76-77,2009.
18. Y.M. Greshishchev, J. Aguirre, M. Besson, R. Gibbins, C. Falt, P. Flemke, N. BenHamida, D. Pollex, P. Schvan, S.C. Wang, "A 40GS/s 6b ADC in 65nm CMOS, "SolidState Circuits Conference Digest of Technical Papers 2010 (ISSCC) , IEEE International,pp.390-391, 2010.
19. K. Doris, E. janssen, C. Nani, A. Zanikopoulos, G. Van Der Weide, "A 480mW 2.6GS/s 10b 65nm CMOS time-interleaved ADC with 48.5dB SNDR up to Nyquist, "Solid-State Circuits Conference Digest of Technical papers 2011 (ISSCC), IEEE International,pp.180-182,2011.
20. J. Harris. (2013,Feb. 17). The ABCs of interleaved ADCs [Online].Available: http://www.edn.com/design/analog/4407107/1/The-ABCs-of-interleaved-ADCs.
21. Z. Cao, S. Yan, Y. i, "A 32m 1.25 /s 6b 2b/step AR ADC in 0.13 m C O , " Solid-State Circuits Conference Digest of Technical Papers 2008(ISSCC),IEEE International ,pp. 542-634,2008.
22. Axim integrated nc. "Demystifying Delta-Sigma ADCs,"Maxim Tutorial 1870, Jan. 2003.
23. N. Maghari U.K. Moon, "A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bi-Directional Single-Slope Quantizer, " Solid-State Circuit, IEEE Journal of, vol. 46, pp.2882-2891,Dec.2011.
24. A.P. Perez, E. Bonizzoni, F. Maloberti, "A 84dB SNDR 100kHz bandwidth low- power single op-amp third-order ΔΣ modulator consuming 140 , " Solid-State Circuits Conference Digest of Technical Papers 2011 (ISSCC).pp. 478-480, Feb. 2011.

