ULTRA LOW POWER AND AREA EFFICIENT OTA FOR PORTABLE AND WEARABLE APPLICATIONS.

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Abstract
A common analogue processing block is the operational transconductance amplifier (OTA). In recent years, the development of OTA with exceptionally low conductivity, low power, low voltage, and better linearity has been mostly used in biological applications. In this project explores the low power consumption CMOS OTA behavior for low frequency or biomedical applications. OTA is to be designed using CMOS 45nm technology with CADENCE virtuoso. The expected power consumption of the device is 20uW with a power supply of 0.7 V.

Keywords: OTA, Operational amplifier, differential pair.

Introduction
A common analogue processing block is the operational transconductance amplifier (OTA). The development of OTA with extremely low conductivity, low power, low voltage, and enhanced linearity has mostly been applied in biological applications in recent years. This research investigates the link between power consumption and CMOS OTA linearity behaviour for low frequency or biological applications that has been described in the literature. The OTA are compared in terms of linearity, technology, supply voltage,power consumption, frequency and their application in biomedical signal processing. Because signals are increasingly being detected in tiny portable wireless devices Low-voltage supply operation is a critical design consideration pulse-oximetry, ECG, PCG, EEG, brain recording, temperature sensing, and blood pressure applications. This paper will help for future Researchers are working to improve linearity and low energy consumption in terms of OTA or biomedical applications. With new initiatives and technology, the field of biomedical electronics is continuously evolving. Biomedical gadgets are now created with a wide range of functions, precision, compactness, and simplicity of use. In Biomedical devices Because of battery life, power consumption has become a critical issue. Depending on the parameters of biomedical signals, portable biomedical designs should give a reduced noise response. Because of the rapid advancement of microelectronics in recent years, an increasing number of applications demand a very tiny amplitude signal measurement module. for example devices implanted for biological uses. Monitoring the biological signals of the human body is an intriguing field of study,because it allows significant information about human health to be gleaned from gathered data. This information is used by doctors to diagnose disorders. Signals in biomedicine such as electrocardiogram (ECG), electromyogram (EMG), electroencephalogram (EEG). Because portable biomedical sensors are often battery-powered, biomedical applications Power-efficient designs are required for devices like ECG and EEG. The ECG and EEG are two of the most critical components of the biomedical system. As a result of these biological programmes, regulate the function of the human heart and brain. Analog Processing cells are required to collect heart and brain activity. These cells use an electrode to attach to the skin and record the activities of the heart and brain. Various integrated circuits (ICs) have been designed for direct activity recording. The low pass filter is the most significant component of these chips. The low-pass filter for the ECG and EEG has a cutoff frequency of 250 Hz or 200 Hz. Examples of filter implementations include Gm-c, Active RC, OTA-C, and a switched capacitor. Filters may be chosen based on frequency requirements. Gm values in the nA / V range and greater than 100pF

capacitors make low-frequency design challenging to implement. Many foundries are unable to supply capacitor values more than 50 pF, owing to the enormous area of a large-scale condenser, which is difficult to accomplish. Another issue with low nA / V steepness is that it is exacerbated by noise, distortion, and imperfection.

The demand for the transportable and easily handle applications has been increased due to low power maintainance. This brings great attention in the world to make use of those applications widely. Subthreshold supply-voltage IC design has recently been studied with the goal of lowering power consumption. The rising demand for power-efficient solutions in medical implanted or wearable devices, wireless sensor nodes, and other related applications is driving this new trend .In VLSI systems, the operational transconductance amplifier (OTA) is the most commonly utilised analog building block. Because of the well suited nature of the OTA's ,these can be used in mixed signals.When there is no high supply voltage is available then we can use the input differential pair of bulk terminals as inputs.High DC gain is required in some of the cases,at that movement we can use amplifiers with multistage which has effiecient frequency compension method.With use of subthreshold bias bulkdriven (BD) transistors is one of the most promising technologies to building analogue and mixed-signal LV LP circuits Because the transistor has a low transconductance in the weak inversion region, and because of the headroom voltage, the standard cascode transistor structure cannot be employed for high output impedance Wearable technology is an electronic device as a fashion ornament, in garments, implanted in the body, or tattooed on the skin or "wearables." Microprocessors power these hands-free gadgets, which also have the ability to send and receive data over the Internet. For the most part, wearable technology development appears to be focusing on more specialised and practical applications. Wearable and implantable medical devices are the two categories of biomedical equipment. The fast advancement of technology in the area of downsizing of electronic devices enables the construction of more adaptive, dependable, and wearable electronic devices, leading to a global shift in health monitoring systems.

Review of Literature

Hyung The use of 0.18 mm CMOS technology has been suggested for An integrated circuit with Medical implants with low-power capacitive feedback amplifiers. The suggested neural amplifier achieves 40 dB voltage gain and 4.3 Vrms integrated input noise from 1 Hz to 10 kHz using a 1 V supply voltage. Noise efficiency is 3.07, and the integrated circuit of the designed amplifier is 0.136 mm 2 [2].

Applications for Moulahcene ECG low voltage and low power ECG control were demonstrated using a two-stage amplifier design It is possible to use this two-phase amplifier in biomedical equipment and compact battery devices with Miller correction (CMRR and PSRR) [3].

A 0.90um CMOS process is used to implement the SPECTRUM-designed circuit. We use N-channel input devices with a P-channel load to reduce amplifier noise as flash noise is lower. ECG amplifier with low noise, CMRR of 131dB, and energy consumption of less than 3uW, as well as outstanding sincerity for heart health, was reported in our study.

Telnaz Zarifi noted that as people become more interested in real-time personal medical monitoring, The need for home medical equipment that is both complex and efficient is on the rise. Non- invasiveElectroencephalography (EEG) is a non- invasive technique used to forecast epileptic seizures and computer-brain interface (BCI). A circuit with extremely low energy consumption is an essential component of the EEG monitoring system. This article shows how to build an EEG signal amplifier.This amplifier is 90 nm CMOS. 1 P 9 M requires 3.6 W of power and 0.048 mm 2 of active area. To tailor the bandwidth to the EEG signal, low-frequency cutoffs of less than 0.1 Hz and high-frequency cutoffs of 10 kHz are used. Using the authentic EEG data collected with the Emama Res EEG-1100, the amplifiers are emulated. Figure depicts an ideal low- power, low-power amplifier for tiny EEG control systems. This CMOS 1 P 9 M 90 nm amplifier uses 3.6 mW at 1.2 V. [4].

dwin said the worldwide need for medical monitoring is rising. The circuit's low-power and low-voltage features must be addressed. It is used to monitor personal health and to prolong the life of a battery. In this work, Edwin presented a biomedical amplifier for detecting ECG impulses. Design includes an HPF and a computation filter. It has a transistor amp (OTA), two linear amplifiers with variable gain, three low-pass filters, and another OTA (ORA). Particularly VGA and LPF make advantage of log compression technologies. [5].

Chinmayee A novel Design includes an HPF and a computation filter. It has a transistor amp (OTA),Input and output cascade structures are folded in this circuit to create a current feedback topology. This aids in the detection of extremely low common mode voltage [6]. The earlier approach, presented by Rakhi [7] enhances The capability of the digital circuit to operate at lower voltages decreases power consumption. We require an analogue interface module like the front end since all physical signals are analogue in nature. A low-pass filter with a cutoff frequency of 250 Hz is built using a mass-driven operational transconductance amplifier with local common mode feedback. A capacitance multiplier is used to further lower the cut off frequency.

The OTA (operational transconductance amplifier) topologies

Low-power OTA topologies are implemented using OTAs. Input and output voltage amplifiers are referred to as OTA. Increasing the amplifier's current efficiency is made possible by the slope gm, which is correlated to the iDS drain current.

designs with a low frequency Neurons interact with one another and generate a neural signal that may be utilised to assess brain function. Include People with locked limbs may effectively use alternative prostheses because to modern integrated circuit technology's close monitoring of these signals. Non- invasive brain wave recording (EEG) is the most often used non-invasive method for collecting cerebral activity.

A.Operational Transconductance Amplifier

Today's biomedical sector requires low noise and low power amplifiers for processing biological signals with tiny amplitudes and low frequencies. Operational Transconductance Amplifiers are ideally suited for these applications (OTA). The OTA symbol is seen in the picture to the right.

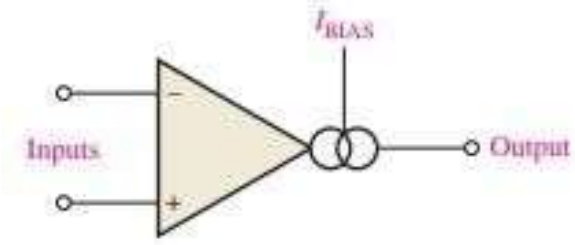

Fig 1.OTA

The OTA is an amplifier. that generates an output current from a differential input voltage. A device that transforms input voltage to output current is known as an OTA. As a result, It is a current-controlled voltage source (VCCS). It is denoted with the sign gm. In the equation, the difference between the inverting and non-inverting voltages represents the output current. Video, intermediate frequency, and radio frequency applications are the most common uses of OTAs. Io = gm(V+-V-). Sample-and-hold, timers, multiplexers, broadcast gear, and high-speed data gathering devices are only a few examples of other OTA applications.There is frequently an extra current input to regulate the transconductance of the amplifier. The OTA, like a typical operational amplifier, features differential input stage with high impedance and may be used with negative feedback .The operational transconductance amplifier is a fundamental component of any electronic system. The function of the transconductor is to convert the input voltage to output current.Symbolic representation at the output end denotes the output current source which depends on the bias current.Similar to normal operational amplifiers the OTA comprises of 2 Differential inputs have

high impedance and CMRR. Unlike operational amplifiers there is bias current input connection exists in the OTA large value impedance at an output and there is no fixed open-loop voltage gain. Like voltage- controlled current sources (VCCS), OTAs are a kind of ideal transistor. OTAs, on the other hand, stay largely steady with temperature since the fluctuation of current with temperature retains the transconductance. An OTA, like a transistor, has three terminals:

- an input or base with a high impedance
- the current output or collector
- a low-impedance input/output or emitter

Although bipolar transistors are used in the majority of units, field effect transistor units are also manufactured. Because its output is a current, the OTA is not as helpful as the conventional op-amp in the overwhelming majority of typical op-amp operations. One of its primary applications is in the implementation Variable frequency oscillators, filters, and gain amplifier stages are difficult to build using op-amps. The graphic below shows an inverting amplifier with a set voltage gain representing an OTA circuit.

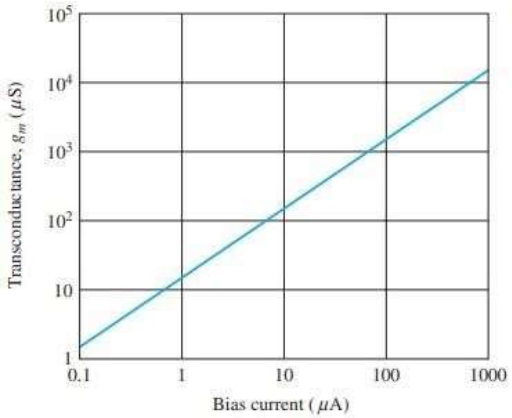

Fig 2. Transconductance versus bias current graph for a typical OTA

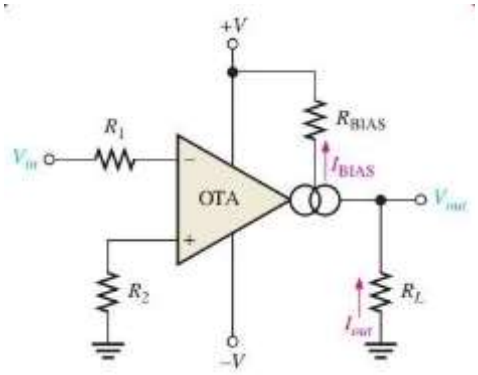

Fig 3. OTA as an inverting amplifier with a fixed voltage gain.

The transconductance and load resistance values are used to alter the voltage gain value.

$$Vout = IoutRL$$

If we divide both sides with Vin then we have.

$$Vout/Vin = (Iout/Vin)\ RL$$

As Vout/Vin is the voltage gain and Iout/Iin is equal to gm, the voltage gain is Vout/Vin.

$$Av = gmRL$$

As shown in the fig 3 below, the bias current and bias resistance determine the amplifier's transconductance.. RBIAS
The most fundamental characteristic of OTA is the ability to alter the voltage gain by changing the bias current.

Operational Amplifier

An operational amplifier amplifies the input signal. Operational amplifiers are high-gain DC-coupled electronic voltage amplifiers with one output. There is a huge variation in output potential between the two input terminals of an operational amplifier. A mathematical operation like as addition, subtraction, integration, or differentiation is performed by an operational amplifier. One kind of differential amplifier is the operational amplifier. Other amplifiers include fully differential, instrumentation, isolation, and negative feedback.

Fig 4. Operational Transconductance Amplifier

It is a high gain, direct-coupled amplifier with a frequency range of 0 to 1 MHz that utilises feedback to alter its general response properties, such as gain and bandwidth, by adjusting the feedback. The op- gain amp's is shown at zero Hz.The input stage is a balanced output differential amplifier with twin inputs. This stage supplies the majority of the amplifier's voltage gain while also establishing the op- input amp's resistance. The output of the first stage powers the second stage of the op-intermediate amp's differential amplifier stage. Dual input unbalanced output is the norm. DC voltage at intermediate-stage output is much above ground potential due to the use of direct coupling. As a result, a level shifting circuit is utilised to lower the dc level at the output to zero with respect to ground. In most cases, the output stage is a complementary push-pull power amplifier. The output stage enhances the output voltage swing and the opamp's current providing capabilities. It also has a low output resistance. Because of its mathematical processes, an operational amplifier is also known as an op-amp. Op-amp is the term given to it.

Symbol:

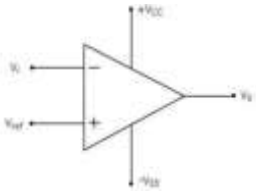

Fig 5. symbol of op-amp

The inputs of an amplifier are inverting (-) and non-inverting (+). Operational amplifiers ideally magnifies the difference between two inputs. Vout is the operational amplifier's output.

$$Vout = AoL[V(+)-V(-)]$$

Where AoL is open loop gain of amplifier

Design of two stage operational amplifier

This is the first stage, which is a differential amplifier pair with an active current mirror. With the current source transistor, the second stage is an active loaded amplifier. The operational amplifier circuit built by It is a direct-coupled amplifier with a wide frequency range.

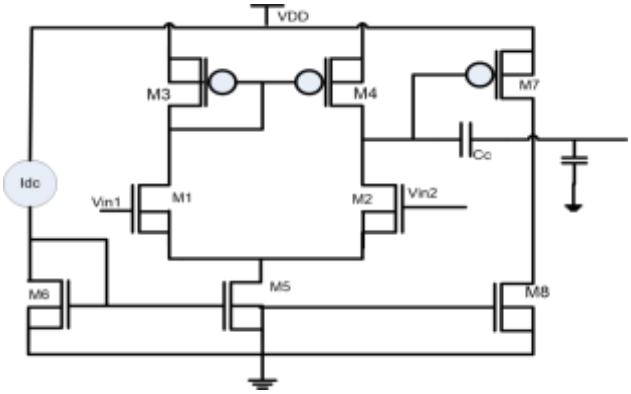

Fig 6. Two Stage Operational Amplifier

Circuit Operation**:**

A. First Stage:

The two-stage operational amplifier is included. The transistors M1, M2, M3, and M4 make up the first stage of a differential amplifier. The transistors M1 and M2 are NMOS. M3 and M4 are PMOS transistors. The transistor terminal M1 and M2 are supplied with Vin+ and Vin-input voltages. The M1 gate does not reverse the input and M2 gate reverses the input. The new mirror is M3 and M4. According to differential stage gain, there is a differential input signal across both input terminals. This rise in this step is the transfer of M1 times to the overall output resistance seen in the drain of M4**.**The primary resistors for the resistance to output are input transistors and load transistors M3 and M4 output resistors.There are three key advantages in this circuit, the current active charging mirror used. The first step is to crate wide output resistance active loading equip ment, which delivers little chip area. The second curre nt topology provides the difference between the input signal and the one-end transition.

Formula:Av1=-gm1*(r04||r02)

gm1=gbw*2π*Cc..Eq2

The difference is accomplished by using current mirror M3 and M4 for single-ended conversion. The M1 current is M3 and M4 mirror and the M2 current is subtracted. The single ended output voltage is provided by multiplying the distinguishing current from M1 and M2 by the input stage output resistance. It is the second stage.

B.Second Stage:

Second phase is a common phase source. The second phase aims to achieve an additional profit made up of M6 and M8 transistors. The second stage takes its input from the differential amplifier stage's output. The output from the drain of M4 is given in this stage and is improved by the standard source configuration via M6. This stage uses a M8 active system to serve as the load resistance for M7, similar to the differential amplifier. The benefit of this stage is M6's transconductance, which is the active load resistance of M6 and M8. Gm2 and Rout are given transconductance and output resistance for the second stage.

Formula

Av2=-gm6*(r06||r08).....Eq3

gm6= 2*2gbw*2π*Cc Therefore overall gain

Av=gm1*gm6 (ro4||ro6)*(ro6||ro8)

Av=(gm1*Rout1)(gm2*Rout2)

Techniques used in this paper

A.Low power Technique (Sleep Transistor Technique)

Biomedical and low-power applications may benefit from a two-stage transconductance amplifier developed in this study employing methods such as sleep transistors and MTCMOS. The schematic of a CMOS inverter is shown in Fig 7. As can be seen, Pull-up pMOS transistor (T1) and nMOS transistor (T2) are included in the circuit (T2). It is possible to achieve the output voltage Vss (typically 0) by setting the input voltage Vin equal to the differential voltage Vdd and vice versa. Because the logic level of the input is reversed by this method. An inverter is a kind of circuit. Conventional practise has it that CMOS circuit leakage current is reduced by using an NMOS sleep transistor to pull down and a PMOS sleep transistor to draw up. A CMOS inverter is seen in the fig 7. There is an NMOS sleep transistor and a PMOS sleep transistor coupled in the pull-down and pull-up paths, respectively. A sleeping inverter is seen in the image. Consider slow inverter performance. When the system is running normally, the sleep signal slp and the complementary sleep signal slpb are both kept at logic 1 voltage levels. As a standard inverter, the circuit is made up of transistors M1 and M2. Aside from transistors M3 and M4, node VG is at ground and node VP is at VDD during normal operation. Consequently, the output of the inverter is inverted. The signal slp is set to logic 0 and the signal slpb is set to logic 1 while the inverter is in sleep mode. Transistors M3 and M4 are turned off as a consequence. Virtual ground and virtual power potentials now exist for node VG and node VP, respectively. Consequently, the inverter shuts off. The potential VG increases while the potential VP decreases as a result of the M3 and M4 transistors being turned off. A increase in transistor M1's source- to-body potential causes the threshold voltage to rise. As a result, the sub-threshold current of transistor M1 decreases. The potential levels at VG and VP are determined by the size (W/L) of the stacked sleep transistors.

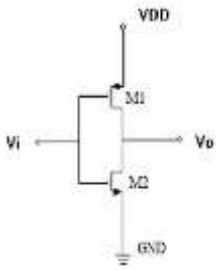

Fig 7. Inverter

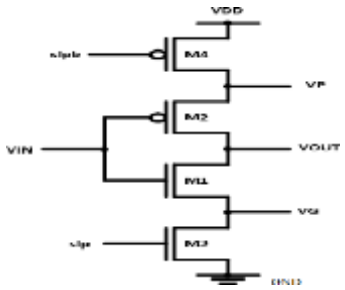

Fig 8. Sleepy Inverter

B.MTCMOS Technique

Multiple threshold voltage (Vth) transistors are used in MTCMOS to minimise a CMOS device's latency or power consumption. When the gate voltage of a MOSFET hits a specific level, the transistor conducts an insulating layer (oxide) is formed at the interface between the transistor and its substrate (body). As a result, the use of low voltage devices is advantageous.

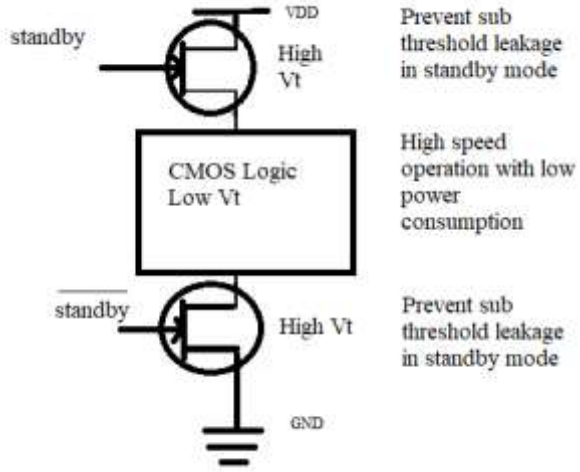

Fig 9. MTCMOS circuit

Although MTCMOS logic is an excellent standby leakage control approach, it is challenging to implement due to sleep transistor size being highly reliant on circuit block discharge cycles. By overcoming the inherent inefficiency of MTCMOS and its scaling issues, they exhibited dual Vt domino logic. By utilising high-Vt cells, leakage can be reduced, and low-Vt cells may be used to boost speed. The MTCMOS technique makes use of both types of cells. To reduce switching power consumption and propagation delay, logic gates with low Vt transistors may operate in active mode by turning off transistors with high Vt. In standby mode, high-voltage transistors are off, blocking low-voltage circuits. In standby mode, high-Vt sleep transistors lower MTCMOS leakage current. Active-to-sleep-to-active mode transitions waste energy in typical MTCMOS circuits. Virtual lines and sleep transistors' parasitic capacitances lose energy when charged and discharged. Virtual power and ground lines have a high capacitance due to wire parasitics, the large number of transistors sharing a single sleep transistor, and decoupling capacitors for voltage stability against bouncing. The parasitic capacitance of virtual lines is increased due to the larger size of sleep transistors, which are required to fulfil performance requirements. In ordinary MTCMOS circuits, mode transitions waste a considerable amount of energy. This paper proposes a novel charge-recycling MTCMOS circuit that enables energy-efficient switching between active and idle modes of operation.

Proposed Operational Transconductance Amplifier

OTC amplifiers are popular analogue processing blocks (OTA). Biomedical applications have widely used low-power, low-voltage OTA with better linearity. The objective of this research is to develop CMOS OTA behaviour with reduced power consumption for low-frequency or biological applications. OTA is to be designed using CMOS 45nm technology with CADENCE virtuoso. The expected power consumption of the device is 160uW with a power supply of 1V.

Two Stage Operational Transconductance Amplifier Design.

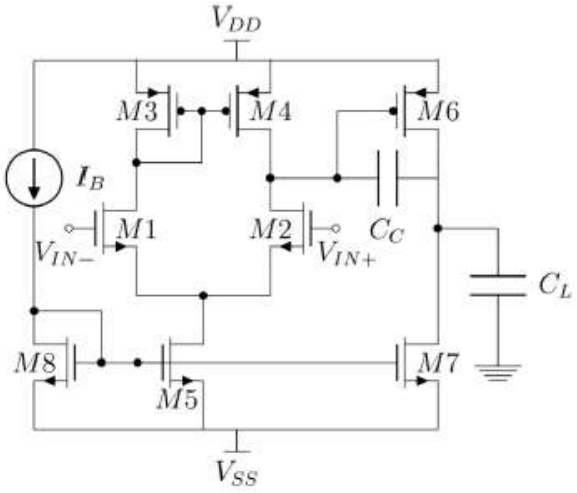

Fig 10. Proposed OTA

A.PROPOSED OTA

Using 45 nm technology, power and area are combined. Transconductance amplifier functioning is determined by the output of an ordinary operational amplifier. Improved phase margin does not necessarily result in greater response in a two-stage amplifier[6]. The output of a transconductance operational amplifier is current, while the output of a conventional operational amplifier is voltage.

The schematics of this speaker is displayed in Fig 10. The Miller OTA is made by an info differential pair and an ongoing mirror with dynamic burden in the primary stage. The subsequent stage is made by an inverter intensifier. Between the first and second stages is associated a remuneration capacitor for soundness purposes. This plan has 12 plan free factors: W1, L1, W3, L3, W5, L5, W6, L6, W7, L7,IB and CC I. Power dissemination is set as plan unbiased and the excess determinations are plan requirements. The outcomes show that all imperatives are met and the power dissemination for the circuit is advanced to drive.

Operational Transconductance Circuits for filtering, instrumentation, and control, as well as neural networks and analog-to-digital converters and comparators, all need amplifiers. [7] Static or dynamic power consumption is possible in CMOS devices. The switching of transistors causes dynamic power consumption, while static power consumption occurs in the absence of transistor switching. By combining PTL and GDI techniques in VLSI design, we may create half adders and full adders that are For both space and electricity conservation [8,9]. As a comparison, this operational transconductance amplifier will be used. and several techniques to comparator design will be employed. Power consumption, speed, and circuit complexity will vary depending on the technique [10]-[12]. On this study, we explain the design of an OTA amplifier in 45nm technology. The following are represented by the paper. An amplifier with three stages is called a two- stage amplifier. An output buffer serves as a last stopgap before the differential amplifier stage.

I .Differential Amplifier Stage

The Differential amplifier stage is made up of CMOS transistors M3, M4, M1, and M2, as depicted in Fig10. M1 and M2 are NMOS transistors, with the gate functioning as a node for differential input. M1's gate input is inverting, but M2's is not. The differential amplifier's PMOS transistors M3 and M4 will reflect current from M1. The current passing through the transistor M2 will be reduced by the amount of reflected current. The differential input signals are converted into single ended output signals using this reflecting topology.

II. Bias Stage

The Bias stage of the architecture, as shown in the fig 10, is constructed by the NMOS transistors M3 and M4 current mirrors, which supply a voltage between the source and gate terminals of M5. M8ise diode is coupled such that both work in the saturation area. The remaining transistors'

necessary biassing is determined by their node voltage.

III. Output Buffer Stage

As indicated in Fig 10, this stage is made up of transistors M7 and M6. This step will increase the amplifier's gain. This stage's input will be the output of the differential amplifier stage. When the output resistances of M7 and M6 are multiplied together, the output resistance of M7 will be multiplied by M6's transconductance.

OTA parameters

This project involves slew rate, power dissipation, gain margin, common mode rejection ratio (CMRR), phase margin, and gain bandwidth.

A. Slew Rate

The rate at which the output voltage varies per unit change in time is what it is defined as in this context. slew rate is expressed in volts per second.
Slew Rate = 2π f.V Where
f=the highest signal frequency, Hz V = peak voltage of the signal.

B. Power Dissipation

Power dissipation is equal to the sum of the total dc power supplied and the power transferred to the load by the device.

C. Common Mode Rejection Ratio

It connects the differential voltage and common mode voltage amplification stages. Ideally, the CMRR number should be zero.

D. Unity gain bandwidth

When the open loop gain equals unity, it is known as the frequency range.The opamp cannot create any further gain beyond this range.

E. Input common mode voltage range

Below are the voltage ranges where an operational amplifier (OTA) would not work effectively. Consequently, this number must not be surpassed in order for an operational amplifier to perform properly.

F. Common Mode Gain

Common mode gain is sometimes called CMVA.One way to think about common mode gain is to think about how the output voltages are related to each other as a function of how much power is being sent into each of its outputs.

Comparision table

Table No.1: Comparision table

Parameter	Base paper	In this work
Supply Voltage	1V	0.7
Technology	45nm	45nm
Gain	30dB	74dB
CMRR	74dB	88dB
Power	68uw	20uw
Unity Gain BW	22MHz	36Mhz
Phase margin	61deg	170deg

OTA Applications

A. Amplitude Modulator

- The fig 11 below shown define the OTA linked as an amplitude modulator. The voltage gain

changes with the application of modulation voltage to bias input.

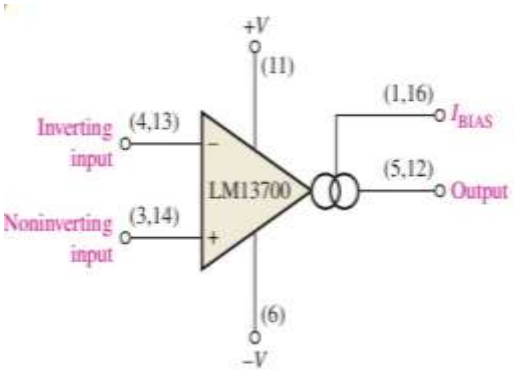

Fig 11.LM13700 OTA

When the constant value of amplitude input signal is given The modulation voltage at the bias input will cause the The output signal's amplitude may be modulated. Gain depends on bias current and modulation voltage, according to this formula's description of how it works. IBIAS = (VMOD – (-V)– 1.4 V)/ RBIAS This modulation process is seen in the picture above for a sine wave input voltage with a high frequency and a sin modulating voltage with a lower frequency.

B. Schmitt Trigger

The below figure indicates OTA in Schmitt trigger arrangments. At high enough input voltages, the Schmitt trigger becomes a comparator with hysteresis, and the module becomes saturated. Saturated output states are activated The trigger point is activated when the input voltage reaches a threshold. if the input value falls below a certain threshold the component changes its state to saturated condition.For OTA Schmitt trigger the threshold level and is adjusted by the current with the use of resistance. In OTA, The maximum output current is equivalent to the bias current. IoutR1 indicates a positive threshold value or higher trigger point in a saturated output condition. When the input voltage surpasses this threshold, the output voltage becomes very negative. That would constitute -IoutR1. Since Iout = IBIAS, the bias current may regulate the trigger points.

Results

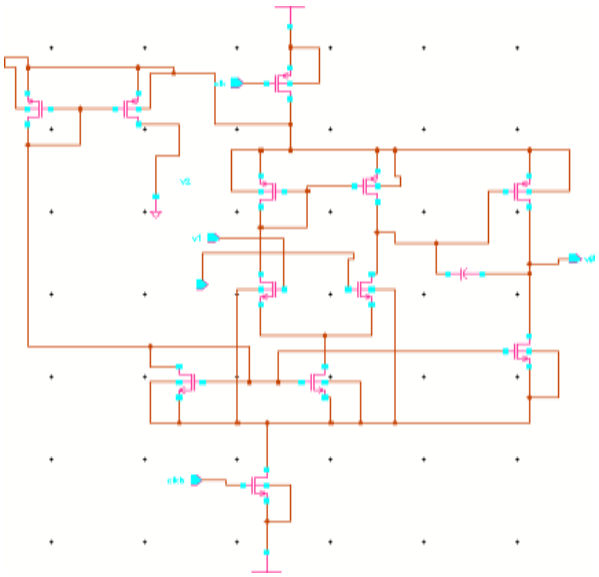

Fig 12. Schematic of overall OTA

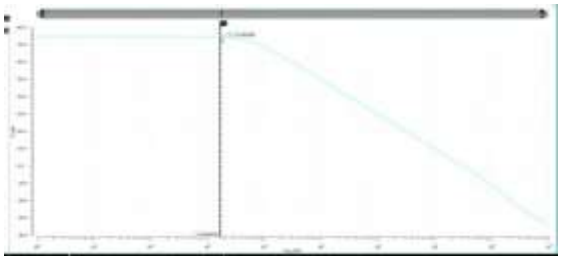

Fig 13. Gain of operational Transconductance amplifier

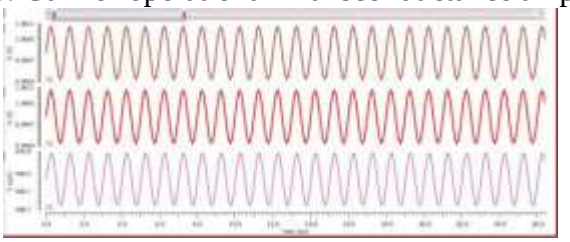

Fig 14. Transient analysis of OTA

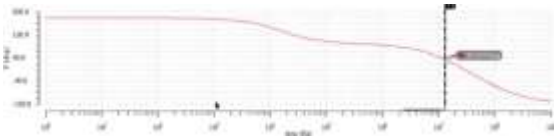

Fig 15. Phase Margin

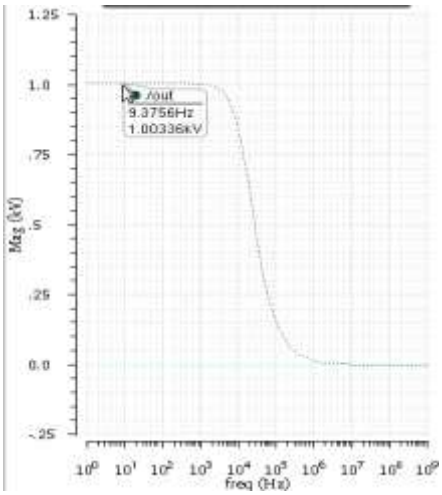

Fig 16. AC analysis

Conclusion

This project has an OTA with a power supply of 0.7V and a power dissipation of 20W. (uW). We may utilise the suggested circuit for a variety of low voltage, low power applications. In this project we apply sleep transistor technique aspect ratio adjustment to minimize the power dissipation and to improve the gain OTA is designed using CMOS 45nm technology with CADENCE virtuoso.

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