A LOW-POWER HIGH-SPEED GDI BASED HYBRID FULL ADDER

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Abstract: In this project Using 45 nm CMOS technology and the CADENCE tool, we proposed a new hybrid FA design in this project that aims to increase speed while minimising power consumption. The simulation results of the design are compared in terms of power dissipation, propagation delay, and power consumption per bit (PDP). Our proposed FA design has the lowest propagation delay and power dissipation over the simulated supply voltage range and the frequency range, according to simulation findings.
Keywords: Full adder, Operational amplifier, GDI technique.

Introduction:

The most common arithmetic operation is addition, and adders are a fundamental component of practically all digital CMOS VLSI systems, including DSP processors, microprocessors, GPUs, and others. The foundational component of a multi-bit adder, multiplier, subtractor, etc. is the Full Adder (FA). The performance of the FA typically affects the system's overall performance because it is on the critical path of the system.

We are living in the era of electronics, and the demand on high performance and energy efficient portable devices are increasing exponentially. As a result, low-power circuit blocks are receiving increased attention in the electronics sector, allowing for the development of long-lasting battery-operated devices. [1{3]. While incorporating this advantage, a device should also work at higher frequencies, to provide the high throughput necessary for most of the modern computation intensive applications. Addition is one of the basic arithmetic operations, and a multi- bit adder circuit implements this operation. Multi-bit adder is an integral part of almost all digital VLSI systems, and is generally part of the Arithmetic and Logic Unit (ALU) inside the micro-processor. . Full Adder is the fundamental building component of a multi-bit adder circuit (FA). FA is used to implement additional operations in addition to addition, such as subtraction, multiplication, address creation, etc.

The FA typically comes into the critical path of the system in all of these processes, and the system's entire success is reliant on the FA's performance.

Figure 1.1 displays a basic block diagram of FA. It has two outputs, Sum and Cout, and three inputs, A, B, and Cin. The binary values at inputs A, B, and Cin are added by FA. Output Sum (LSB) and Output Cout (MSB) are terms for the addition's Least Significant Bit (LSB) and Most Significant Bit (MSB), respectively. Table 1.1 shows the input-output relationship (truth table) of the FA.

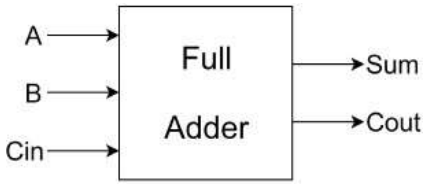


Figure 1: Full adder block diagram

Inputs			Outputs	
A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1 Input-output relationship of the FA

LITERATURE :

In the composition, various dynamic/domino CMOS FA schemes were suggested or discovered. The data capacitance is reduced by these FA circuits' usage of high speed NMOS semiconductors and a small number of PMOS semiconductors, which are typically required by the clock signal. From this point forward, dynamic/domino CMOS FA plans can achieve high speed divergence compared to static CMOS FA plans.

However, a major drawback of the dynamic/domino CMOS design is the high power dissipation caused by the excessive clock load and stupid trading out of stuff mode. Similar to how static CMOS design is less resistant to leakage current than dynamic/domino CMOS design, Dynamic/domino CMOS FA designs are therefore inappropriate for battery-operated devices. [2].

The static CMOS design consumes low power diverged from dynamic CMOS plan; accordingly FAs arranged using static CMOS style are more sensible for battery worked devices [2, 3]. The static CMOS FA plans can be further sub-arranged into _ve general characterizations: standard CMOS reasoning style, pass-semiconductor reasoning style, Complimentary Pass-semiconductor Logic (CPL) style, transmission doorway reasoning style, and mutt CMOS reasoning style. The standard CMOS reasoning style relies upon two indispensable associations: the PMOS pull-up network and the NMOS pull-down network [2, 4, 13].

The strength of the conventional CMOS reasoning style against voltage scaling [2] is a key component of reliable movement at low voltage. Additionally, it has a short rising/falling period, allowing it to operate at higher frequencies [2, 13]. Higher data capacitance, which might hinder the introduction of the FA, especially when connected in flood, is a problem with standard CMOS logic [2]. The conventional CMOS FA schemes are partially depicted in [4, 8].

The FA uncovered recorded as a hard copy, with the most un-number of semiconductors, is arranged using pass-semiconductor reasoning style, and it requires only 6 semiconductors to make yields Sum and Cout [14]. Other FA plans proposed using pass- semiconductor reasoning style, also require just 8 to 10 semiconductors [15{19]. All around, FA arranged using pass-semiconductor reasoning style, requires less number of semiconductors, and hence, achieves low power dispersal [19]. The critical disadvantages of these FA plans are lamentable driving limit and cutoff voltage drop, which make these FA arrangements unacceptable for chain and tree structures [2, 13].

CPL style relies upon two absolutely irrelevant NMOS associations. FA arrangement considering this style can achieve quick, feeling free to have, incredible driving limit due to result inverters. One such FA design using 32 semiconductors is represented in [8]. Nevertheless, this FA design consumes high power due to bundle of internal center points [2]. In like manner, more number of semiconductors consumes greater silicon district and eccentric game-plan of semiconductors

increases design unpredictability [2].

An unusual type of pass-semiconductor circuit is the transmission entry reasoning style, in which NMOS and PMOS semiconductors are equivalently related. Combining NMOS and PMOS semiconductors results in the reasoning regard with almost little restriction voltage drop since the entrance terminals of both semiconductors are controlled by free signals. By including more NMOS or PMOS semiconductors in the FA scheme, the transmission entry reasoning style resolves the edge voltage drop (of the pass- semiconductor reasoning style) problem..

A hard copy itemised portion of the pass- semiconductor based FA plans [1, 20, 21] can achieve fast speed and full voltage swing with minimal power consumption (different from conventional CMOS and CPL styles) [2, 8]. These FA plans are appropriate for chain and tree architectures, provided that bu ers are only sometimes utilised to increase the sign strength [2]. By concentrating on reducing the number of semiconductors while maintaining awareness of the sufficient driving limit and speed, the cross variety CMOS reasoning style achieves the benefits of static CMOS setup methods [2, 3, 22].

In the past two or three years, various crossbreed CMOS FA schemes were suggested and recorded in hard copy to achieve low Power-Delay-Product (PDP)1 [2, 3, 13, 22–34]. The majority of the time, FAs are used to create multi-bit two-operand adders (such as the Ripple Carry Adder (RCA), Carry Select snake (CSL), Carry Skip snake (CSK), etc.), as well as to build multipliers (such as the Braun, Baugh- Wooley, and Booth) that rely on multi-bit multi- operand snake (suggested as Carry Save Adder(CSA)) [35]. This statement implies that the multi-bit two-operand adders have a chain topology.", which requires fast time of Cout in each FA, to accelerate convey expansion in the chain of streamed FAs, and todecrease fizzles [13].

This statement implicitly refers to the multipliers' use of CSA trees (for adding various lacking things) as "tree structures." Here, the FAs work together to create a tree (model, Dadda or Wallace Tree [36]), where each layer primarily creates total and convey vectors, and the final complete and convey vector passes via a Carry Propagation Adder (CPA)2 to provide the expansion's reaction [13]. In tree architectures, it is crucial to quickly execute both the Sum and Cout results in each FA. Power distribution and speed are accorded equivalent weight when assembling battery-operated devices [2, 3].

High speed, little power dispersal, extraordinarydriving strength, and full voltage swing at yield are requirements for a decent FA plan. The transmission entry and cross variety CMOS design styles are more appropriate for battery operated devices out of the FA setup styles that have been explored up to this point, and FAs structured using these styles can achieve low PDP respect in chain and tree topologies.

Because of the significance of a FA in the information way and memory address age; portrayal of FA is important for the enhanced plan of current frameworks [13]. In writing, some information test designs were recommended [37{40] to assess power dispersal, greatest engendering delay and to check the right usefulness of the FA plan. Paper [37] examines the drawbacks of ordinary info test designs utilized for portrayal of FA plan, and how it will prompt wrong assessment of force scattering and greatest spread delay. Likewise, a similar creator proposed their new information test design in [40] for right assessment of force scattering, most extreme engendering delay and to check the right usefulness of the FA plan.

HYBRID ADDER :

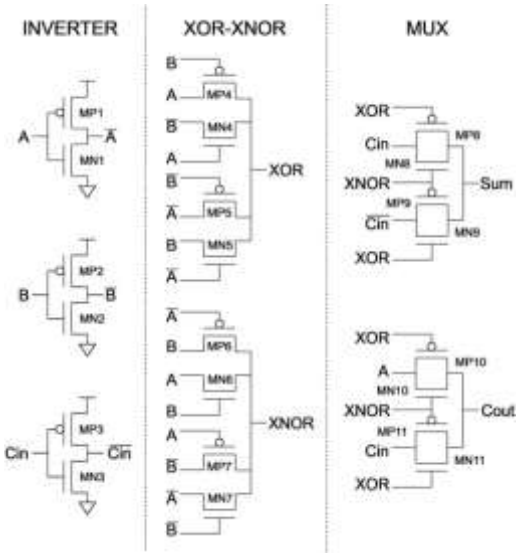
Two new cross breed CMOS FA plans, alluded to as Low Power Hybrid Full Adder" (LPHFA) with 22 semiconductors and 18 Transistors are proposed inthis part. Both the FA plans have three phases: Inverter, XOR-XNOR and Multiplexer (MUX).

3.1 Inverter Stage

For the XOR-XNOR and MUX stages, the inverter stage generates the necessary modified input signals. In the LPHFA FA scheme, semiconductor matches between MP1-MN1, MP2-MN2, and MP3-MN3 individually create A, B, and Cin. While Cin is utilised in the MUX stage to create Sum, An and B signals are employed in the XOR-XNOR stage. Additionally, in the LPHFA FA

scheme, MP1-MN1 and MP2-MN2 semiconductor matches independently create only B and C in signals.

Fig 2 Schematic of hybrid adder with 22 transistors



To control the decision line of a 2-input transmission doorway type multiplexer, this step generates the XOR and XNOR signals (in MUX stage). In the LPHFA and LPHFA FA designs, we designed the XOR-XNOR stage using two different approaches. We focused on reducing the expansion time in the LPHFA FA plan by concurrently sending the XOR and XNOR signals (which later go to the MUX stage as assurance line). Double Pass Semiconductor Logic (DPL) is used to deliver both signs (XOR and XNOR) [46]. In an LPHFA FA plan, the following Boolean conditions are employed to create the XOR and XNOR signals.

XOR = AB + AB (LPHFA: MP4-MP5-MN4-MN5).

XNOR = AB + AB (LPHFA: MP6-MP7-MN6-MN7)

In LPHFA plan, we zeroed in on decrease in power dissemination. Diminishing power dispersal by lessening the quantity of semiconductors in the design is conceivable XNOR signals.

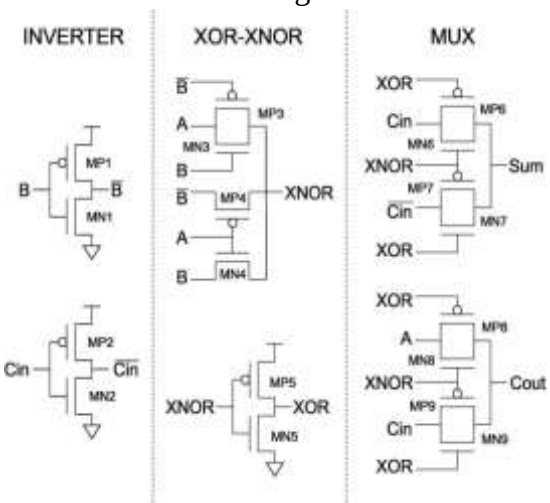


Fig 3 Schematic of hybrid adder with 18 transistors

A XOR-XNOR configuration proposed in [3], and alluded to as the invertible inverter and transmission entryway XNOR [4], is utilized in LPHFA plan, and it comprises of 6 semiconductors, which is two semiconductors less when contrasted with XOR- XNOR planned utilizing DPL style (8 semiconductors). Likewise, plan recommended in [3], doesn't need A sign, consequently, one less inverter is required in the Inverter stage. By and large, 4 semiconductors can be chopped down from the plan, at the expense of nonconcurrent age of XOR and XNOR sign, and this might increment engendering deferral of the FA. Following Boolean conditions are utilized to produce XOR and XNOR signals in a LPH.

FA plan:

XOR = XNOR (LPHFA: MP5-MN5)
XNOR = AB + AB (LPHFA: MP3-MP4-MN3-MN4)
MUX Stage

Transmission entryway type multiplexers are usually used to produce yields Sum and Cout in numerous FA plans [1, 3, 23, 25, 33, 47]. The reproduction results in [30], shows that, the FAs planned utilizing transmission entryway type multiplexers, by and large accomplishes lower PDP values. Subsequently, both our FA plans contain transmission entryway type multiplexer to produce Sum and Cout. The XOR and XNOR signals created from XOR-XNOR stage are utilized as choice line of the multiplexers. Cin and Cin are contributions of the multiplexer that creates Sum, and Cin and An are the contributions of the multiplexer that produces Cout. Last Boolean articulations for yields Sum and Cout are

Sum = Cin(A`B) + Cin(AbB) (LPHFA: MP8-MP9-MN8-MN9)
(LPHFA: MP6-MP7-MN6-MN7)
(LPHFA: MP8-MP9-MN8-MN9)

3.2 Simulation Environment:

Our proposed FA plans are contrasted and ten existing transmission door plans. All FAs are planned and reproduced in Cadence Virtuoso utilizing 045nm library Test bed utilized for reproduction of FA configuration is displayed in Fig 4. Here, input inverters are going about as driver, and creates sensible information signals. Inverters at the result side are going about as a result load. Working condition considered for reproduction is as per the following: temperature = 50XC, supply voltage = 1V, input driver strength = 2× inverter (least size1) and yield load = 8× inverter (least size).
Semiconductor widths of all FA plans are improved to accomplish low PDP for picked working condition.

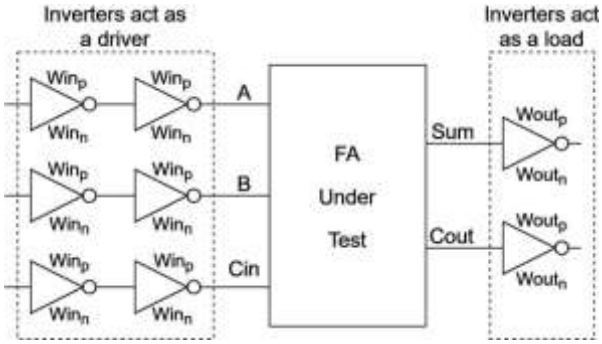


Fig 4 Reproduction of FA configuration

Existing transmission door and half breed CMOS FA plans. The outcomes are displayed in climbing request of PDP. The LPHFA FA configuration can accomplish most reduced PDP esteem contrasted with other 11 FA plans. That's what the explanation is, LPHFA FA configuration has the least engendering delay for yields Sum and Cout contrasted with other FA plans. The power scattering of LPHFA is higher contrasted with other 7 FA plans (20T ordinary, Kamsani, LPHFA, TFA, TG CMOS, Yen and Zavarei), however generally speaking result of postponement and power (PDP) is the least. Our other proposed FA plan (LPHFA), has a higher PDP esteem contrasted with 5 FA plans, however it figured out how to accomplish low power dissemination contrasted with 10 other FA plans (just TFA has lower power scattering contrasted with LPHFA). As we can see from Table 3.1, FA plans with lower number of semiconductors will generally accomplish low power dispersal. Yet, such FA plans, can't decrease engendering delay (generally because of nonconcurrent age of XOR and XNOR signals. i.e., TFA, TG CMOS, LPHFA, Yen). On other hand, FA plans with bigger number of semiconductors are neither ready to accomplish most reduced spread delay, nor least power dispersal (i.e., Mariano, Milad, SMIC). Thus, such FA plans will generally have higher PDP esteem. FA plans, which have sensible number of semiconductors (around 20 to 22 semiconductors) and are likewise ready to create XOR and XNOR signal all the while, can accomplish low PDP esteem (i.e., 20T ordinary, Kamsani and LPHFA). Thus, FA plans with adjusted engendering postponement and power dispersal qualities, figured out how to accomplish low PDP esteem.

Proposed framework:

A Low power Hybrid Full Adder (HFA) is proposed by conveying Pass Transistor Logic (PTL), CMOS rationale and transmission door (TG) rationale on the Cadence Virtuoso stage in 45-nm innovation. Different modules, in particular the XOR module, the convey generator module, total generator module are executed for acknowledging 1-digit HFA. An inverter rationale is utilized close to the XOR rationale to get the rationale of XNOR which is expected for planning the proposed HFA. The engendering delay (tpd) and normal force of the circuit are to be 20 ns and ~10 μWseparately, at 1V inventory voltage.

The proposed framework plans full snake circuit utilizing Gate dissemination Input (GDI) strategy. Utilizing this procedure one can plan a computerized circuit with low power in implanted framework. The quantity of semiconductors utilized in the circuit is least consequently they are utilized by the circuit is diminished as well as the deferral and power utilization.A combinational circuit known as a full viper performs the three-piece math problem. Expansion of ideas over a basic mathematical exercise and justification for sophisticated signal handling. The first two bits of the data sources are An and B, which are referred to as operands. The third info bit Cin is a bit that was brought in from a previous, less-critical stage. The output bits, total and complete, are the results of expansion activity and will be used to convey information to the next stage.

expansion activity, and the articulation: The proposed plan comprises of 16 semiconductors counting two XOR door cells to create aggregate and one multiplexer cell to deliver complete, as displayed in figure , the block graph displayed in figure, and reality table of proposed full snake introduced in tableI.

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 2 Truth Table Of Proposed Full Adder

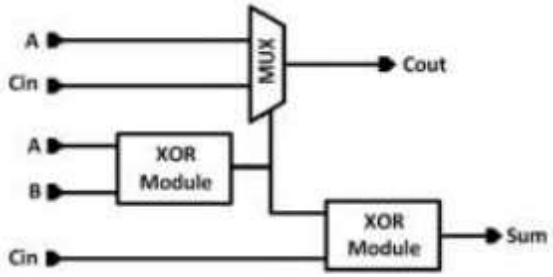


Fig 5 Block Diagram For Proposed Full Adder

The significant advantage of utilizing GDI procedure is that countless capabilities can be carried out utilizing this strategy. We can see from the table 2 that GDI can be utilized for carrying out different plans like MUX, AND, OR and so on. The most intricate plan among these is the planning of MUX, which should be possible utilizing 2 semiconductors. Though utilizing other regular procedures it requires 8-10 semiconductors for planning a MUX. The fundamental disadvantage of GDI procedure is that of swing corruption. This is because of edge misfortune and to dispense with this we need to utilize silicon on cover or twin-well interaction to understand, which is pricey. Planning a full viper the significant structure block is XOR entryway utilizing GDI method.

3.3 Outline of GDI approach:

This section provides a brief overview of Gate- Diffusion Input, one of the most popular computerized resoning techniques now in use. The GDI technique can recognise a variety of complex rational abilities using just two semiconductors. The basic cell shownin Fig 6 is used as the basis for the GDI reasoning. Although the cell's design resembles that of a static CMOS inverter, there are a few significant differencesto be aware of.

The GDI cell has three inputs: Pinput to the source/channel of the PMOS, G-normal contribution to the PMOS and NMOS, N-contribution to the NMOS's source/channel, and Body terminals of both the NMOS and PMOS are with no obvious end goal in mind one-sided in GDI by associating with the data sources N and P, separately.

The GDI system was initially presented for manufacture in Silicon on Insulator (SOI) and twin- well CMOS processes. Afterward, standard CMOS viable GDI cell was presented it was shown that the greater part of the rationale capabilities like AND, OR, XOR, and MUX are mind boggling which require 6-12 semiconductors to carry out utilizing traditional static CMOS and transmission entryway rationale, however a similar rationale capabilities can be carried out with just two semiconductors utilizing GDI cell by basically changing the data sources. Table 1 shows the rationale table for carrying out different Boolean capabilities utilizing GDI and Table 2 shows the semiconductor count examination between the GDI and traditional CMOS executions of various Boolean capabilities. F1 and F2 are the two general rationale capabilities presented by GDI which can be utilized to acknowledge other complex capabilities more effectively than the all inclusive NAND and NOR rationale doors

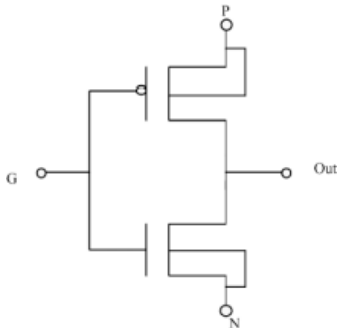


Fig 6 Basic cell

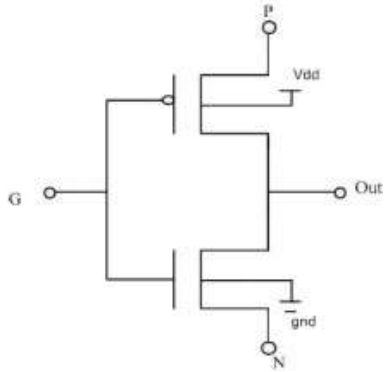


Fig 7 Structure of a basic gate diffusion input (GDI) cell with inputs G, P, and N.

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'0'	'1'	A	$\overline{A}$	NOT
B	'0'	A	AB	AND
'1'	B	A	A + B	OR
C	B	A	$\overline{A}B+AC$	MUX

Table 2 Implementation of various boolean functions using GDI cell

4. PROPOSED FULL ADDER : Proposed cross breed full snake plan as a general rule, the rationale elements of an essential 1-cycle full viper can be addressed as in (1) and (2) Only 14 semiconductors are needed for the suggested entire snake arrangement, as shown in Fig. 3. It mostly consists of five logic blocks that were planned using the MVT-GDI method Two multiplexers, one Swing Restored Transmission Gate (SRTG), one Swing Restored Pass Transistor (SRPT) block, one XOR/XNOR, and two multiplexers roundout the circuit. The GDI technique is used to plan the XOR/XNOR block.. Since the way of the inverters utilized in the XOR/XNOR blocks has no voltage drop, they are consolidated with standard VT gadgets. Since

the GDI MUX-1, multiplexes the result of theXOR (A ⊕ B) and the XNOR (A XNOR B) with a control input (Cin) to get the aggregate capability. Inthis way, the (3) can likewise be addressed as in (3). The convey yield (Cout) is produced by the GDIMUX-2, which multiplexes the data sources Cin andB with control line from the result of XNOR rationale(A XNOR B). Hence, the (2) can likewise beaddressed as in (4).

$$C_{out} = (\overline{A \odot B})C_{in} + (A \odot B)B$$

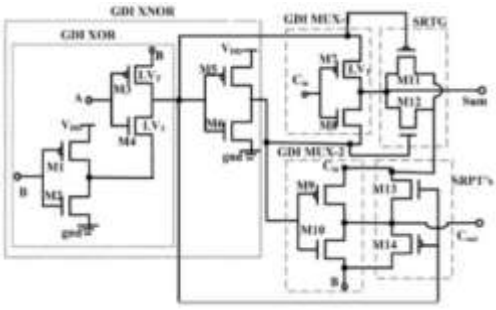


Fig 8 Proposed full adder

Be that as it may, the proposed structure appears to be like numerous past XOR/XNOR rationale based plans and creators' past GDI-based plan, however none of the past plans gives full rationale swing just 14 semiconductors. In the proposed plan, the going all out is guaranteed utilizing a SRTG at the result of the total and SRPT's at the convey yield (Cout). It can be seen that the swing rebuilding semiconductors (M11, M12,M13, M14) are 'ON' when there is a VT drop at the result of thesum age GDI MUX1 and Cout age GDI MUX-2 to provide going full speed ahead rationale. Since there is no VT drop at the result deepest of the cases as expressed in Table 4, the semiconductors (M11, M12,M13, M14) are likewise consolidated with standard VT semiconductors.

RESULTS : CADENCE simulations based on 45nm technology were run in order to examine the performance of the suggested circuit, and its performance was compared to that of other full swing full adders. All full adders have been programmed to operate at a frequency of 20MHz. assessed average power consumption. The average power consumption is the average circuit power consumption taken into account for multiple cycles and all conceivable input combinations. Of the four full adders, the GDI-H full adder consumes the least amount of power at all supply voltages. At lower supply voltages, it is obvious that the C-CMOS has the least latency. Comparing full adders from HPSC and Hybrid-CMOS, the GDI-H full adder exhibits the least amount of delay at all supply voltages. The full HPSC.

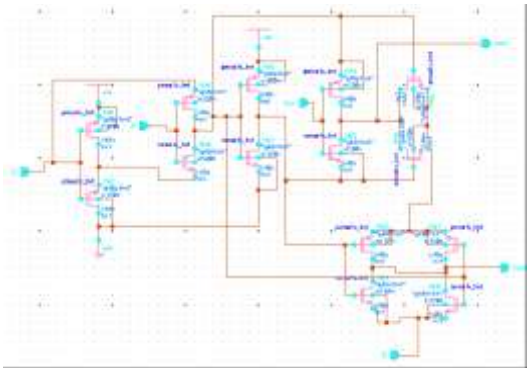


Fig 9 Schematic of Hybrid full adder

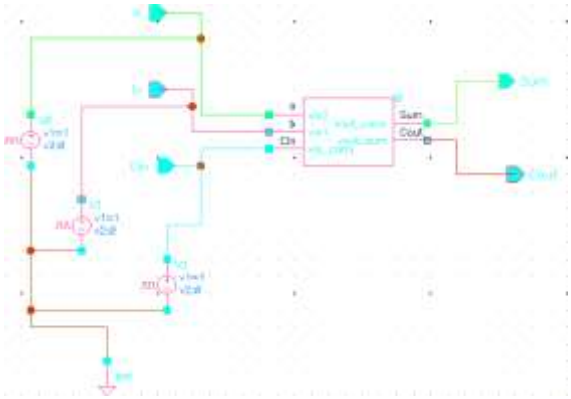


Fig 10 Hybrid full adder test bench setup

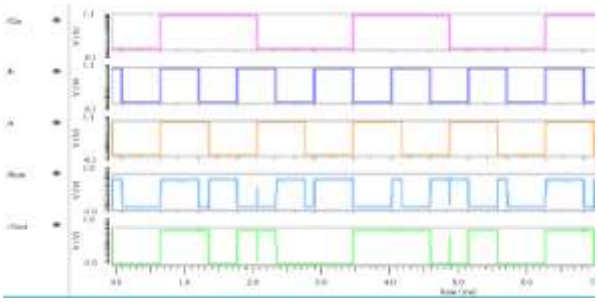


Fig 11 Hybrid full adder simulation results

COMPARISION TABLE:

Full Adder	No. of Transistors	Power(nW)
C-CMOS	28	2.91
HSPC	22	1.97
Hybrid-CMOS	24	2.20
GDI Hybird	18	1.22

Table 3 comparision table

CONCLUSION :

This project involves designing three hybrid full adders. To lessen the GDI threshold voltage issue and improve the driving capabilities for cascaded operation, this design uses full swing XOR, OR, and AND gates logic. The faster functioning and lower voltage are made possible by the improved driving capability, which ultimately leads to less energy use. Using the Cadence tool, the aforementioned designs are simulated, and a power analysis is completed.

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