DESIGN OF LOW POWER 7T SRAM CELL USING FOR FPGA APPLICATIONS

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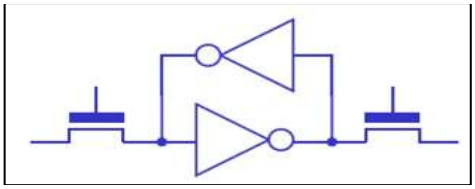
Abstract

Memory is the important part of most of the electronic systems but the major problem with the design of memories is performance in terms of speed and power dissipation. In this paper performance for read and write operations of SRAM cells based on different configurations are compared, specifically in each cell design the static-noise-margin (SNM) is calculated by observing butterfly characteristic curves. According to the result analysis the 7T SRAM cell in 45nm CMOS technology has less power dissipation and power delay product since it uses single bit for both read and write operations. The total circuitry is designed and simulated by using Cadence virtuoso and spectre respectively.

Keywords: SRAM, Bit-line, Low Power, DTMOS, SNM, Latch, CMOS Technology.

Introduction

As the technology of memory on Systems-on-Chip (SoC) is shrinking, the devices and embedded systems are emerging, so the low power consumption is very essential for the system design. Static Random Access Memory (SRAM) contains more than 70% area of the Soc. A standard 7T SRAM cell has two-bit lines for read and writes operation thus it consumes more power. There are many techniques for power reduction like scaling of supply voltage (Vdd) and threshold voltage (Vt), multi-Voo, multi- Vt etc. Scaling of voltages affects adversely on the stability of the SRAM cells. In this paper a dual Vt 7T (seven transistor) SRAM cell is proposed and compared with the standard 6T SRAM cell based on read delay, write delay, leakage power consumption and Static Noise Margin (SNM) (during hold, read and write). This proposed cell uses single bitline for read and writes operation. Thus it also improves the access time of the cell. The consumption of leakage power is reduced by 61.50%. Write delay is reduced by 67%. All the simulation work is carried out using the Eldo SPICE tool of Mentor Graphics on 65nm technology at 27 0 C. Random Access Memory is accessed by an address, but its latency is independent of the address. Static Random Access Memory (SRAM) is the volatile kind of i.e., it retains its data as long as the power supply is given while the Dynamic Random Access (DRAM) should be periodically refreshed. An SRAM cell is used to store single bit information in the form of either '0' or '1'. SRAM is used in cache memory. From the last more than five decades the size of the CMOS devices is being scaled down to accommodate maximum memory on Soc. More memory that means more information can be stored, that makes the system faster. The low power operation of system can be achieved by lowering the leakage current which can reduce the leakage power consumption. For this purpose, supply voltages and threshold voltages are being scaled down but it affects the stability of SRAM cells that is the noise margin is reduced. Shrinking of technology also degrades the stability. This paper is organized as- first section covers read and write operation of conventional 7T SRAM cell. In second section the proposed dual-Vt 7T SRAM cell is discussed. Third section has the parameters to be compared. Simulation is shown in fourth section and finally conclusion is given. Rapid development of low power, low voltage SRAM cells has been experienced during recent years. This is due to an increasing demand of embedded devices, notebooks, laptops, handheld communication devices and IC memory cards. Due to these concerns limiting power consumption is a must and hence new techniques are being realized to improve energy efficiency at all levels of the design. In this paper an overall analysis has been carried-out for a novel SRAM cell with respect to stability and switching power consumption.



1.Single Bit Line SRAM Cell.

In the traditional 7T-SRAM, the cells are expected to be both read stable and also writable and such functionality must be preserved for each cell under worst- case variation. At the cell level, the static noise margin and write margin are both maintained by the selection of calculated transistor strength ratios, which in turn presents conflicting constraints on the cell transistor strengths. For the cell stability during a read operation, the storage inverters are usually made strong and the pass-gates weak. Whereas the opposite is usually the case for cell write ability which is a weak storage inverter and strong pass-gates. Device variations common in Nano-scale fabrication can severely impact this delicate balance of transistor strength ratios, which dramatically degrades stability and write margins. These problems are further exacerbated by low voltage operations as threshold voltage variation consumes a larger fraction of these voltage margins. Variability can thus limit the minimum operating voltage of SRAM.

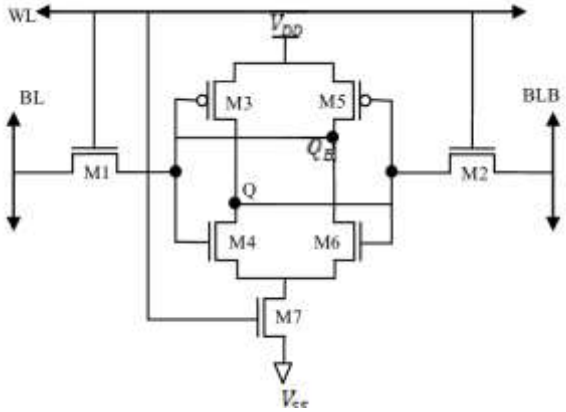


Fig: 2. 7T SRAM

Proposed SRAM

The proposed design has increased the read stability and SNM, without affecting the Size or Power Consumption of a Standard 7 Transistor SRAM cell.

7T Standard Cell

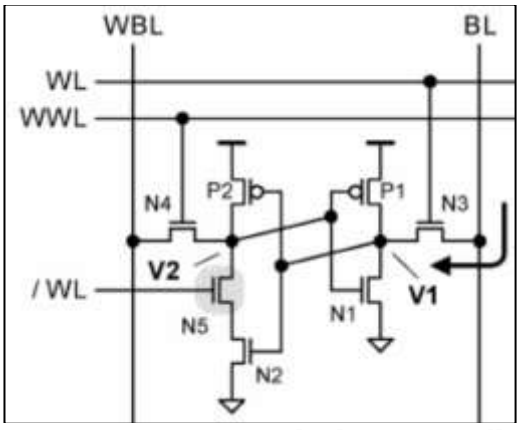


Fig 3. Transistor Standard SRAM Cell

The schematic (Fig: 3 Once again shows the 7 Transistor SRAM cell which uses two bit-lines and one word-lines

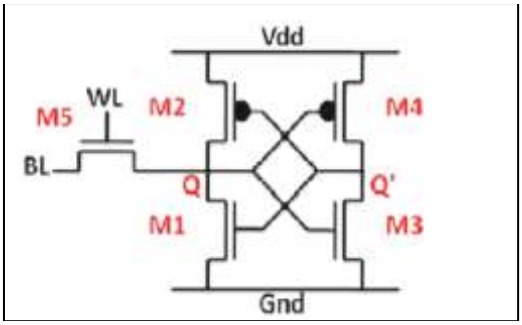


Fig.4 Transistor (Single Ended) SRAM Cell

With the Transistor N3, N5 being taken away a schematic like (Fig 4) is obtained, which still functions like the 7T SRAM, but the advantages of this design are reduction in cell area and power consumption. The cell area decreases by one transistor and one bit line. The power consumption from charging the bit line decreases by approximately a factor of 2 because only one bit line is charged during a read operation instead of two-, and the-bit line is charged during a write operation about half of the time (assume equal probability of writing 0 and 1 instead of every time when a write operation is required.

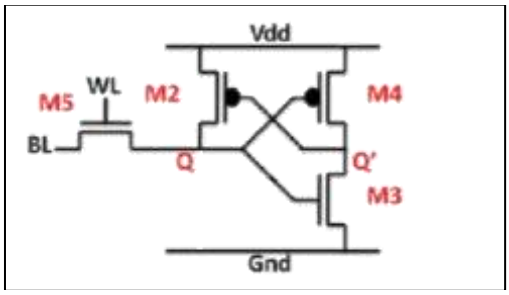


Fig.5 Transistor (Single Ended) SRAM Cell

When the Transistor N2, is being taken away a schematic like (Fig.4). is obtained, which has the functionality of a SRAM, and the main advantage of this design is the further reduction power consumption. Other advantages include significant larger write margin and smaller delay for writing 1, and slightly smaller cell area.

Techniques used in this paper

DTMOS logic

Since few years there is a wide growth of portable devices in market like portable computers, cell phones, low power application devices. Nowadays the important issue is on analog circuit design which consumes low power, low voltage and gives high performance. One major limitation while designing low power circuit and implementing the portable device at lower voltage is threshold voltage (Vth). Therefore, a reduction in threshold voltage is essential for operation of low voltage power devices. one of the best solutions to reduce the threshold voltage is to use the DTMOS technique. Therefore, for reducing the power consumed an effective method is to decrease the power supply voltage (Vdd). So, one of the methods is implementing a CMOS transistor by dynamic threshold voltage (Vth) this is a basic idea of DTMOS technique. When DTMOS transistor is in OFF state it shows high threshold characteristics and leakage current is minimized and when DTMOS transistor is ON state it acts like low threshold device at lower supply voltage for higher current driving capability. This feature makes DTMOS technique to be one of the most appropriate methods for low power and voltage applications.

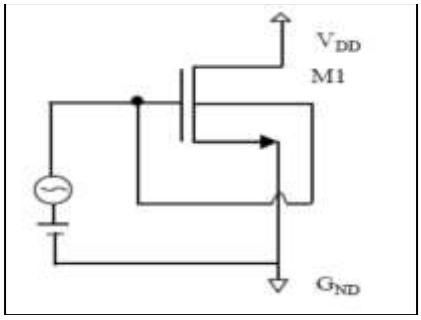


Fig:6. DTMOS transistor

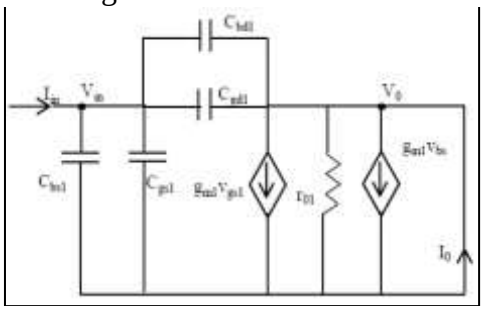


Fig:7 Small signal model of the conventional DTMOS transistor

It has two trans-conductance, the gate trans-conductance (gm) and body trans-conductance (g_{mb}). And the relation between both the trans-conductance is given by [7]

$$\frac{g_m}{g_{mb}} = \frac{C_{BC}}{C_{GC}}$$

where

C_{BC} is the total body-channel capacitance

C_{GC} is the total gate- channel capacitance

In (DTMOS) i.e., "Dynamic Threshold CMOS" a threshold voltage is dynamically changed to outfit the circuit's operating state as shown in figure, here the NMOS and transistor body is biased dynamically based on the variations in the input voltage applied to the gate terminal. The small signal model for the DTMOS transistor is shown in figure. From the figure we can observe that the DTMOS logic is applied to an inverter, sufficient voltage is applied to body of both PMOS and NMOS transistors are provided by the potential dividers (pd) which are coupled to the input of an inverter. In standby mode a high threshold voltage produces a low leakage current, whereas in active mode a lower threshold voltage allows higher current drive. DTMOS technique can be achieved by tying up the body and gate together. Its supply voltage is limited by in built potential diode in silicon technology. A P-N diode is connected in among a body and source, and it should be in reverse biased condition. [8]

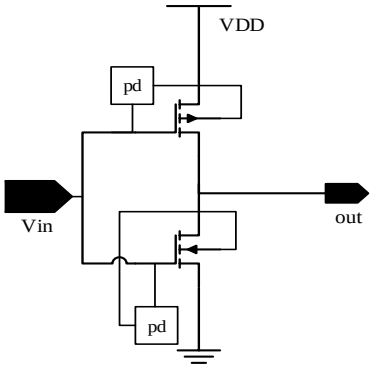


Fig: 8 DTMOS Circuit

The DTMOS technique while in ON state i.e. (VBS> 0) decreases the threshold voltage and also transistor off-state leakage current. After fabrication, by changing the body-source voltage the transistor's threshold voltage can be modulated. In bulk MOSFETs, the V_{TH} is given by:

$$V_{th} = V_{th} + \gamma\left(\sqrt{|2\emptyset f - V_{BS}|} - \sqrt{|2\emptyset f}\,\right)$$

Where
V_{Th0} =V_{th} when V_{SB} = 0,
γ =The body-effect coefficient typically
$\emptyset$ = Fermi – Potential.
V_{SB} = voltage between source and body

The features of an NMOS transistor with and without body biasing are shown in figure. The green line shows that the drain to source current (Ids) with body biasing, and the red line indicates that the drain to source current without body biasing. Here we can observe that, with body biasing the transistor is conducted earlier than the without body biasing, that is the threshold voltage is reduced. [8]

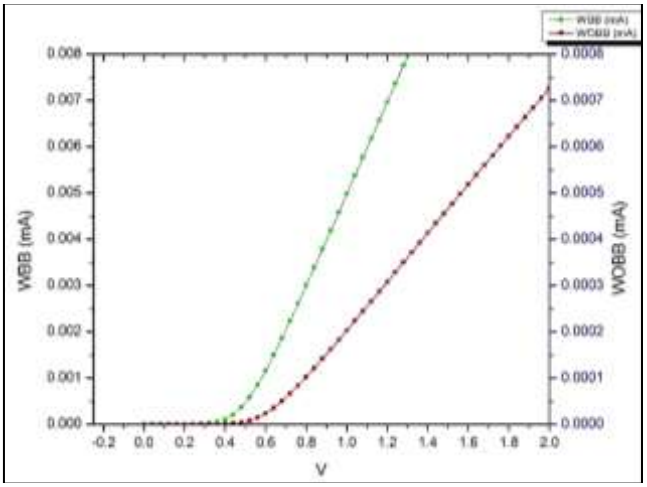


Fig:8 NMOS Transistor characteristics with DTMOS Logic

The proposed 7 Transistor new SRAM Cell is created by adding two more transistors MRA (Read Access Transistor) and MRD (Read Driver Transistor) which shall work independently during read operation and won't affect the Cell SNM in any way.

- **Hold:** If the cell content is a 1 (Q=VDD, Q'=0), both memory nodes will lock each other at their respective voltages. However, if the cell content is a 0 (Q=0, Q'= VDD), Q is floating. the leakage current through M5 must be greater than that of M2 to ensure Q stays at 0. Fortunately, since NMOS (M5) is
  a stronger current driver than PMOS (M2), this condition is satisfied.[2]
- **Write:** The word-line WL is charged to VDD as in 7T Standard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down NMOS for memory node Q allows writing a 1 into the cell easily. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged, and then word-line WL is charged to VDD as in 7T Standard SRAM.[2]
- **Read:** Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is pre-charged to VDD. The read word line RL is then asserted to VDD. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cutoff and the bit line BL would not be able to discharge through MRD to Gnd, and it would read a 1.[2]

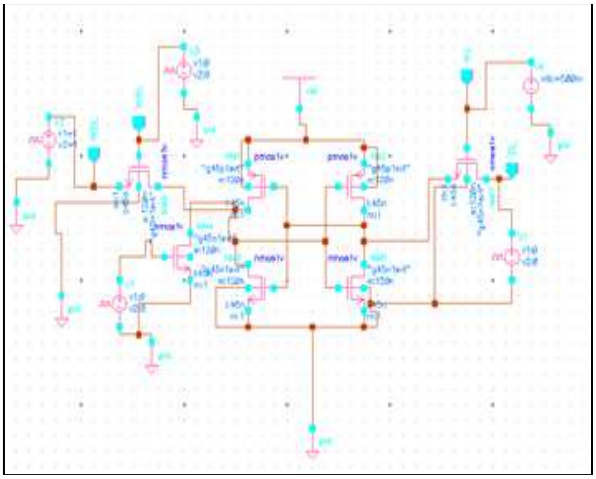


Fig.9. 7T SRAM Cell using Cadence

In an SRAM operation (Fig.9), power is consumed

In two phases:

- Setup phase
- Operation phase.

Energy consumed during the setup phase is dominated by pre-charging or discharging various buses such as bit lines and word lines. Using the formula E line = 0.5 * C line * Vline 2, in which Cline is the line capacitance and V line is the change in line voltage, the energy drawn from the supply by the bus can be calculated. From this information, the average power of an SRAM operation is obtained by dividing the clock period, assuming that each SRAM cell can only perform one operation per clock period, and all word lines and bit lines are discharged to 0 after performing each operation. Also, the clock has 50% duty cycle. In the simulation performed, a clock with 40ns clock period is used (or equivalent to 25MHz clock frequency and 1pF bit-line capacitance).

Dynamic power dissipation can be lowered by reducing the switching activity and clock frequency, but it affects the performance. Reduction of supply voltage leads to degradation of the cell data stability. Hence dynamic power dissipation can be lowered by reducing bit-line capacitance of the SRAM cell without degrading the performance.

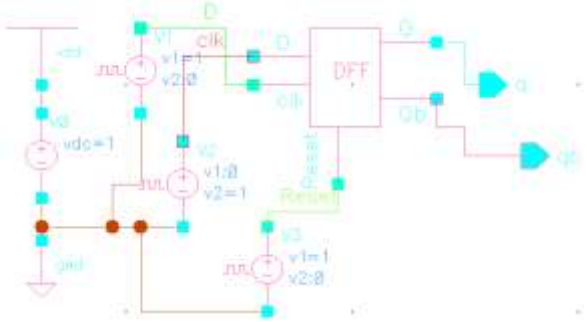


Fig: 10. Test bench of the proposed DFF

Considerable research in understanding and modelling the stability of the SRAM cell has been done in the past. Development of several analytical models of the static noise margin (SNM) have been done in the past. Each of the work tried to optimize the design of the cell, to forecast the effect of parameter changes on the SNM and to estimate the impact of intrinsic parameter variations on the cell stability (Fig.10). Further, maximization of cell stability has been done in new SRAM cell circuit for future technology nodes.

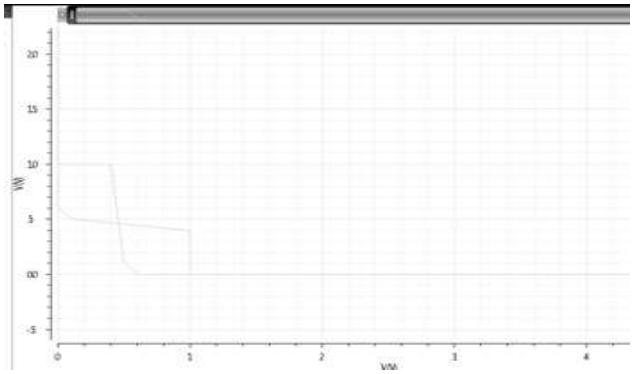


Fig: 11. The SNM Curve plotted for implemented 7T SRAM Cell

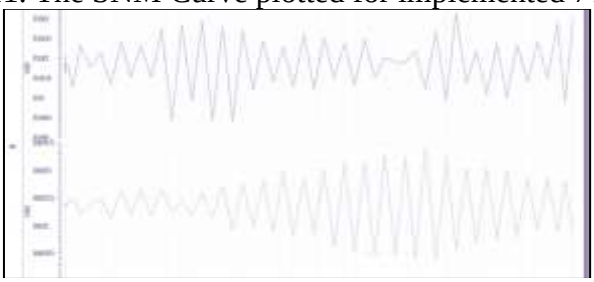


Fig.12. Write 0 Wave form.

Fig.13. Write 1 wave form

3.1. Table: Performance Comparison:

OPERATIONS	7T SRAM Cell	Proposed 7T SRAM cell
WRITE 0	12uW	516pW
WRITE 1	81uW	504pW
READ 0	162uW	6.3uW
READ 1	81uW	5.5uW

CONCLUSION

Continuing technology scaling puts, a limit on how much supply voltage can be scaled. Therefore, limiting the power consumption with new architectures are the design requirements in recent Integrated circuits. In the case of SRAM, one seemingly counter intuitive approach is to utilize only a single bit-line without jeopardizing read stability, which leads to the development of a Single Ended 7T SRAM.

The new SRAM operating scheme gives a significant power reduction by reducing the amount of switching on bit lines. Extending this operating scheme also allows us to propose a single bit line design that achieves a relatively smaller area while retaining all of the power saving advantages. For a small penalty in delay, Single Ended 7T SRAMs are attractive alternatives as memory storage for applications that do not require high clock frequency.

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