BI-DIRECTIONAL CSPWM AND SPWM CONVERTER WITH IMPROVED POWER FACTOR AND HARMONIC REDUCTION TECHNIQUE

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Abstract: This article demonstrates a proposed technique for improving the power factor (PF) of single-stage rectifiers and controlling the load voltage in response to changes in grid voltage and load. To alleviate the above problem, this article offers a novel bi-directional CSPWM (Continuous Switching Pulse Width Modulation) and SPWM (Sinusoidal Pulse Width Modulation) based converter which can improve PF as well as reduce harmonics. This converter is evaluated based on two cases, CASE I: CSPWM based rectification and SPWM based inversion scheme CASE II: Rectification and inversion both operations using SPWM scheme. The proposed control scheme uses two Bi-directional IGBTs and two diodes, which is bridgeless, no need of transformer, and free from output current sensor. The suggested scheme is simulated using MATLAB/Simulink and implemented on DSPic33FJ64mc802 platforms to validate the effectiveness of the proposed approach using two cases for 1KW system. It is observed that the anticipated control scheme provides improved PF (Power Factor), good voltage regulation, minimization in harmonics and THD (Total Harmonic Distortions) as compare to existing systems that enhances the performance of converter.
Keywords: Power Converters, Power Electronics, Electronic Drives

1. Introduction:

Most ac-dc power conversion applications need stabilized dc output voltage with better steady state and transient performance. The capacitor filter based rectifier is simple and cheaper; however, it degrades the supply voltage quality, compromising the performance of other loads linked to it as well as producing other issues [1][2]. To achieve these mandated standards, power electronics researchers are inventing new ways for a superior efficacy interface since the mid-1980s. PF correction (PFC) circuits are the collective name for these new circuits. The power converters are important for micro-grids, smart grids, electrical vehicles, industrial machineries, commercial products, etc [3][4][5].

A single switch rectifier circuit is simplest scheme for hysteresis current control where the hysteresis band is increased [6] [7]. The two switch rectifies have shown significant improvement over the traditional single switch rectifies [8] [9].

The typical AC-DC converter (rectifiers) are designed using diodes but suffers from poor power quality, larger voltage distortions, inferior PF at main input, low effectiveness and bulky nature of AC and DC filters [10]. The VIENNA rectifier generates a DC voltage across the two switches linked to the primary side of transformer, which are represented by [11], [12], and [13]. Even though it only has three switches, the VIENNA rectifier is subjected to more stress than a six-switch converter. The VIENNA rectifier, on the other hand, has concerns with poor current regulation during overload, start-up over current, and inability of bi-directional operation.

In [14] researchers present a single-phase multilevel flying capacitor active rectifier with hysteresis-based control. Controlling the input current allows for PF and output voltage management. When the frequency ratio changes, PLL is employed to determine the phase information of the input voltage that causes transients. The researcher's in [15] proposes a smart charger for electric vehicles that uses three

wire distribution feeders. They used six active switches to accomplish bi-directional flow, which boosts hardware, cost, switching losses, and complexity. An Efficient Grid to Vehicle (G2V) and Vehicle to Grid (V2G) Converter Systems for EV Application was proposed in [16]. Simple bi-directional power line communication (PLC) method by switching ripples in DC-DC converter is proposed [17] in which current ripples in the input side of converters are used as signal carrier whose frequency is modified as a function of transmission data. G2V and V2G applications are the primary goals of this bidirectional on-board single-phase electric vehicle charger. A high gain boost converter and buck converter are the essential components of the bidirectional charger arrangement. The battery state of charge (SoC) is used to charge and discharge the battery [18]. Three MOSFET switches, four capacitors and two inductors make up the converter's topology. Furthermore, by lowering switching losses, the converter's efficiency is improved in variety of applications such as electric vehicles, energy storage systems, distribution generation, and micro grids [19]. The CLLC bidirectional resonant converter (CCLC-BRC) maintains the advantages of the LLC resonant converter, such as high performance and high power density, and provides a symmetrical bidirectional voltage gain, making it suited for scenarios with bi-directional power flows. A small-signal model for the CLLC-BRC was developed using the augmented description function method [20]. Dual active bridge (DAB) dc-dc converters provide a unified phase shift control technique for better transient current response [21]. For grid assistance, a bidirectional charger employed to transfer energy from the battery to the AC side. Furthermore, an active bridge permits synchronous rectification on the secondary side, to minimize conduction losses [22]. Partial differential equations are used to design networks with a large number of components (PDEs). The components count in the network decides the convergence of a sequence. The sequence meets to a range boundary as N approaches infinity, which is the solution of a particular PDE [23]. The efficiency and operation stability of , an isolated bidirectional boost full bridge dc-dc converter using active start-up assisting circuit and an active voltage clamping snubber [24]. A bidirectional three-phase AC/DC Dual-Active-Bridge (DAB) converters is utilized for the high frequency connection based on novel modulation scheme that is realized using sinusoidal line currents and zero voltage switching (ZVS) by exact regulation of phase shift and duty cycle under bidirectional operation [25].
By considering all above literature, it has been seen that there is scope to make system more optimized.

The key contributions for the proposed system are,

1. We achieved the rectifier power factor nearer to unity.
2. We successfully achieved the bi-directional power flow.
3. We stabilized the DC output voltage of rectifier in case of changes in grid.
4. We successfully reduced Total Harmonic Distortions as much as possible (THDs)
5. We are able to Minimized Total Harmonic Distortions by achieving bi-directional power flow (THDs)

This research article provides comparative analysis of two examples (case I- rectification with chaotic sinusoidal pulse width modulation (CSPWM) and inversion with sinusoidal pulse width modulation (SPWM) scheme, case II- rectification and inversion both with SPWM scheme). The converter utilized has no bridges, no transformers, and no output DC current sensors. To take use of the benefits of digital implementation, all of the above methods are executed digitally. The detailed simulation is performed using MATLAB/Simulink, and an experimental setup for a 1KW system is created to validate it.
The rest of the article is arranged as follow: Section 2 elaborates the block diagram and discussions of the suggested methodology in detail. Section 3 provides details about design and modeling of the proposed scheme. Section 4 focuses on the simulation results and deliberations. Finally, section 5 offers the conclusion of proposed work.

2. BLOCK DIAGRAM AND DISCUSSION OF PROPOSED SYSTEM:

2.1 CASE I: rectification using CSPWM and inversion using SPWM scheme

Fig 1. illustrates the schematic of suggested scheme for the CASE I, where rectification operation is using continuous switching PWM and inversion operation is using sinusoidal PWM scheme. In CSPWM scheme only lower switches S2 and S4 of bi-directional converter are operated. Upper switches S1 and S3 are acts as diode to pass current, in order to complete the path of circuit. CSPWM scheme not only give higher PF but used to regulate DC link voltage with very less period of time. This scheme uses DC link voltage as a input called as feedback DC link voltage, base on it all the rectification parameters are achieved.

In sinusoidal PWM scheme all four switches S1, S2, S3 and S4 are used. To achieve positive half cycle of inverted AC signal S1 and S4 switch are ON and for negative half cycle S2 and S3 are activated. The variation in duty cycle to achieve sinusoidal output, value of Kfactor and array value of look-up tables are used. This scheme uses AC line voltage as a input called as VAC feedback, based on it sinusoidal AC line voltage is achieved.

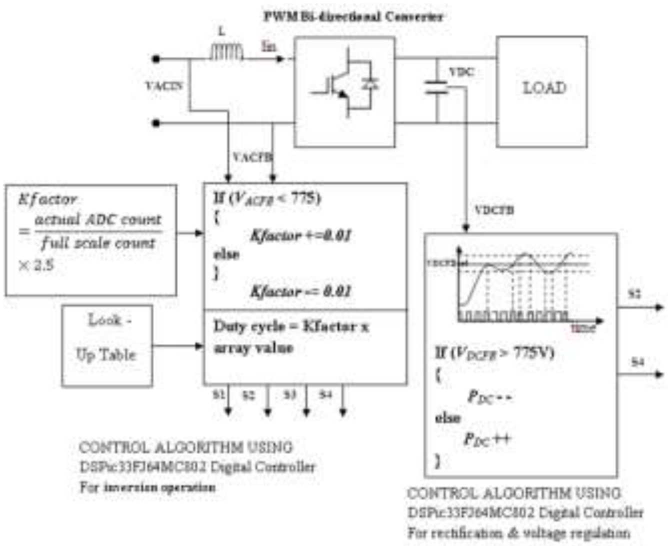


Fig. 1 Block schematic of proposed scheme in CASE I.

2.2 CASE II: Rectification and inversion both operations using SPWM scheme:

Fig. 2 . illustrates the schematic of suggested scheme for the CASE II, where rectification and inversion both operations are performed using SPWM scheme. For the rectification operation only lower switches S2 and S4 of bi-directional converter are used. Upper switches S1 and S3 are acts as diode to pass current, in order to complete the path of circuit. In SPWM scheme duty cycle increases slowly, hence current flowing at the input side is less or it is in the proportion of duty cycle. Due to this the PF of front end converter is less also the time required to regulate the DC link voltage is somewhat more. This scheme uses DC link voltage as a input called as feedback DC link voltage, base on it all the rectification parameters are achieved.

In inversion operation using SPWM scheme all four switches S1, S2, S3 and S4 are used. To achieve positive half cycle of inverted AC signal S1 and S4 switch are ON and for negative half cycle S2 and S3 are activated. The variation in duty cycle to achieve sinusoidal output, value of *Kfactor* and array value of look-up tables are used. This scheme uses AC line voltage as input called as VAC feedback, based on it sinusoidal AC line voltage is achieved. This scheme implemented in same way as implemented in CASE – I inversion.

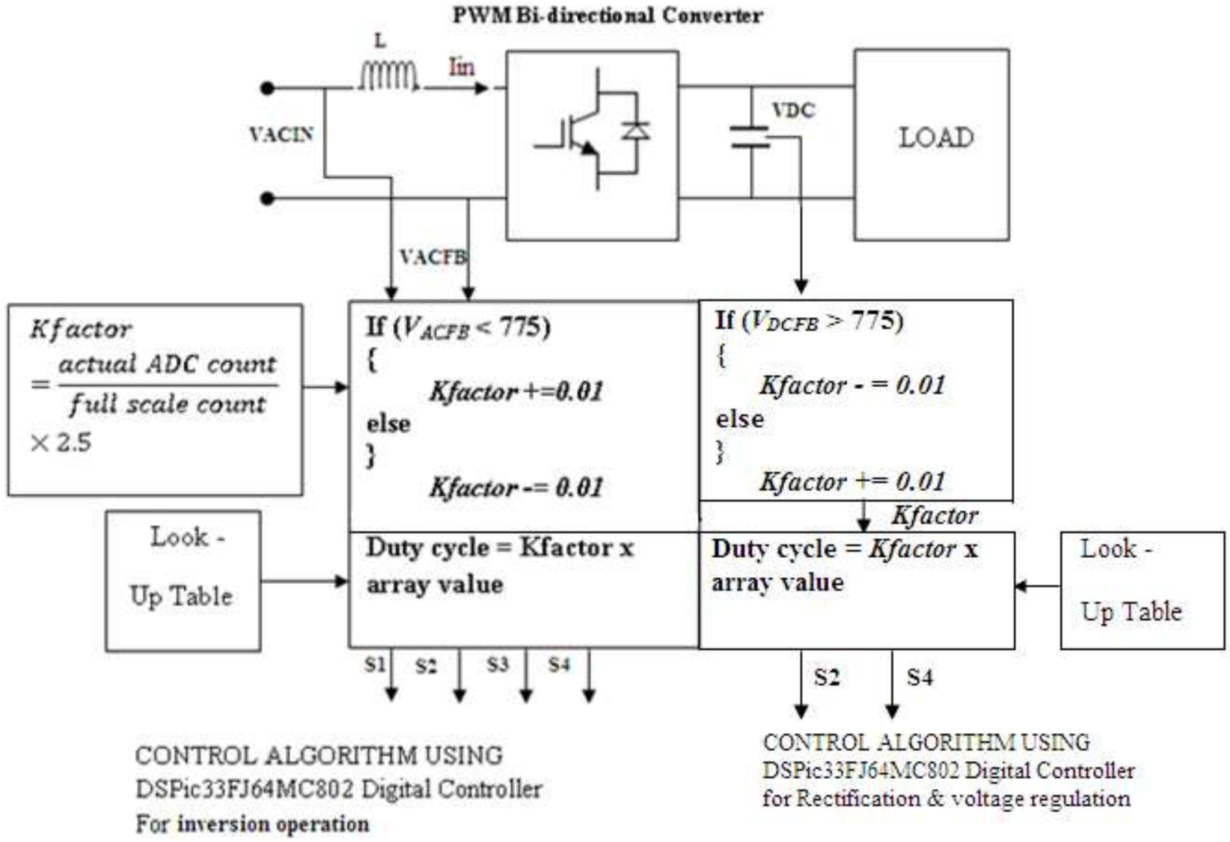


Fig. 2 Block Diagram of proposed scheme in CASE- II

3. DESIGN AND MODELING OF SYSTEM:

3.1 Modeling of switch

The IGBT switch (IRF4G50WD) is used as switch because of its higher switching frequency, and larger current conduction capacity. The IGBT is able to works at higher switching frequency and can handle larger power.

3.2 Modeling of Driver

The IGBT switches are used for the active conversion of voltage sources. Out of two available drivers of IGBT (IR210-International Rectifier and VLA 503 hybrid driver), VLA 503 drive is used for driving the switch because of its distinctive features such as-

1. Better electrical isolation between input and output with help of opto-coupler
2. No need of bootstrap operation
3. Turning OFF the switch due to +15V and -9V provision

3.3 Modeling of controller

The DSPic33FJ64mc802 is employed for the modelling of the proposed controller which is application specific integrated circuits that provides various onboard and inbuilt functions as described in Table 1..

Table 1. Specifications of DSPic33FJ64mc802

Parameter	Specification
ADC	10 Bit
Linear data memory	64 KBytes
RAM	16 KBytes

Flash Program Memory	64 KBytes
Operating Voltage	3.3V
Digital Signal Controller	16 Bit
IC pins	28

3.4 Input inductor Design

The proposed design considers inductor ripple current as 40% of output current as given in equation 1. The inductor ripple current normally lies in between 20% to 40% of the output current. The inductor value is obtained using equation 2.

$$\Delta \mathrm{IL} = 0.4 \times Io \times \frac{VDC}{VINpeak} \quad (1)$$

Where, ΔIL represents estimated inductor ripple current

$$\mathrm{L} = \frac{VINpeak \times (Vo - VINpeak)}{\Delta IL \times fs \times Vo} \quad (2)$$

Here, *VINpeak* represents input voltage
Vo denotes desired output voltage
fs stands for minimum switching frequency of the converter
ΔIL represents estimated inductor ripple current

3.5 Output capacitor Design

The low value equivalent series resistor (ESR) capacitors are suitable for minimization of output voltage ripple. Equation 3 provides the solution for adjusting output capacitor value for desired ripple factor.

$$\mathrm{Cout(min)} = \frac{Iomax \times D}{fs \times \Delta Vout} \quad (3)$$

Where,
Cout (min) represents the smallest output capacitance
Io (max) stands for highest output current required for the application
D depicts the duty cycle
fs provides the lowest switching frequency
ΔVout describes the expected ripples in output voltage which can be calculated using equation 4.

$$\Delta \mathrm{Vout(ESR)} = ESR \times \left\{\frac{Iomax}{1 - D} + \frac{\Delta IL}{2}\right\} \quad (4)$$

Where,
ΔVout (ESR) represents extra output voltage ripple caused by capacitors ESR
ESR stands for corresponding series resistance of the utilized output capacitor (0.1ohm)
Iout (max) denotes highest output current
D defines duty cycle
ΔIL denotes ripple current of inductor

4. RESULTS AND DISCUSSION

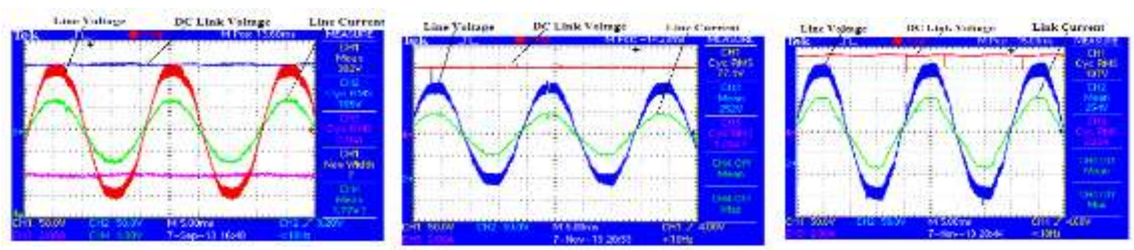
4.1 **CASE-I**The DSPic33FJ64MC802 digital controller is employed for the development of the suggested SPWM based converted using CSPWM technique for rectification and inversion. The simulations are carried out using C language. The simulation and experimentation parameters are summarized in Table 2.

Table 2. Experimental parameter specifications

Parameter	Symbol	Value
Boosted DC voltage	VO	380V
DC link capacitor	C	440µF
Line RMS voltage	VIN	160V
Line frequency	f	50Hz
Load resistance	R	Variable (90Ω - 225Ω)
Input inductor	L	1mH
Switching frequency	fs	20KHz

4.1.1 Experiment Results to indicate PF in Rectification using CSPWM

Simulation results for rectifying mode for different loads are visualized in Fig. 3. Fig. 3(a)illustrates the line current followed by line voltage waveform that indicates the 0.987 PF it is approximately unity at full load condition. At 80% load, some disturbances are appeared in line current but these are negligible. The observed PF of rectifier is 0.979 shown in Fig. 3(b). When the load of rectifier becomes 20% of full load, the PF becomes 0.972 shown in Fig. 3(c). Channel 1 and channel 2is set at 50V/Div whereas channel 3 is at 2Amp/Div.



(c)

(b) (c)

Fig. 3 Experiment results (a) PF for full load condition, (b) PF for 80% load, (c) PF for 20% load and (d) PF for no load condition.

4.1.2 Experiment Results to indicate voltage regulation in Rectification using CSPWM

Fig. 4 displays the output voltage regulation when DC load is changed from 5% to 80% on a regular basis. The experiment result is shown in trace 'a' of Fig. 4; it is perceived that the DC link voltage remains regulated while the load varies from 80% to 5% and back to 80%. The voltage regulation of DC link within a very short amount of time, which was minimal when the load changed. Channels 2 and 4 are set to 50 volts per division, whereas channel 3 is set to 2 amps per division. The step change and time of DC link voltage regulation after a load shift are depicted in trace 'b' of Fig. 4. When the load varies from 5% to 80%, the time/division knob is set to 250msec, indicating that the voltage is regulated for 40ms period, line current enhancement and constantvoltage.

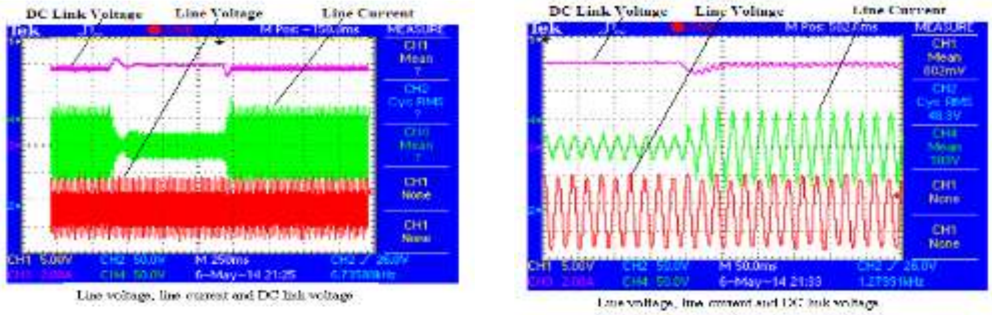
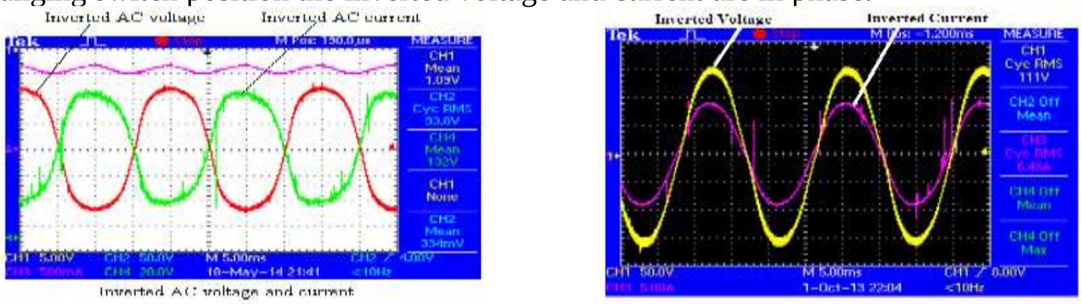


Fig. 4 Experiment results of voltage regulations (a) DC load changes periodically load varies from 80% to 5% and 5% to 80%. (b)) DC load varies from 5% to 80% to show period of voltage regulation.

4.1.3 Experiment Result to show Bi-Directional operation

In order to validate the simulated result of bi-directional power flow, SPWM technique is used for the inversion operation. Fig. 4.3 shows the inversion operation using same converter which is used for the rectification operation. The inverted voltage and currents are illustrated in Fig. 5(a), where voltage and current are 180o out of phase. Trace 1 and 2 of Fig. 5(b) shows the inverted output for different loads, but by changing switch position the inverted voltage and current are in phase.



(a) (b)

Fig. 5 Experiment results of inverter (a) Inverted voltage and current with 180° out of phase (b) In phase inverted voltage and current for 1KW and 500W resp.

4.1.4 Line Current harmonic pattern

Figure 6 depicts the line current harmonic pattern. All lesser order harmonics and third harmonics are completely eliminated, while the fifth and seventh harmonics are minimized to a minor degree.

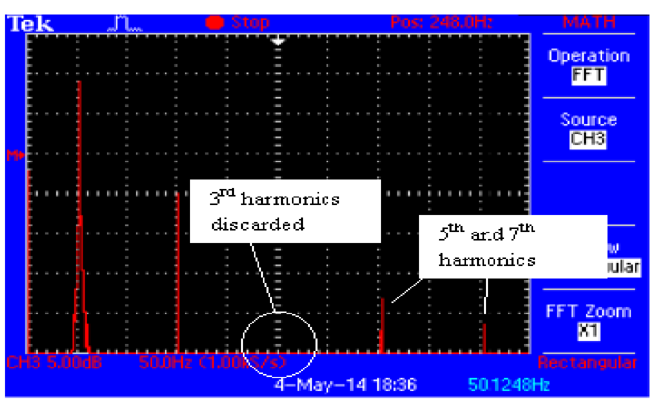
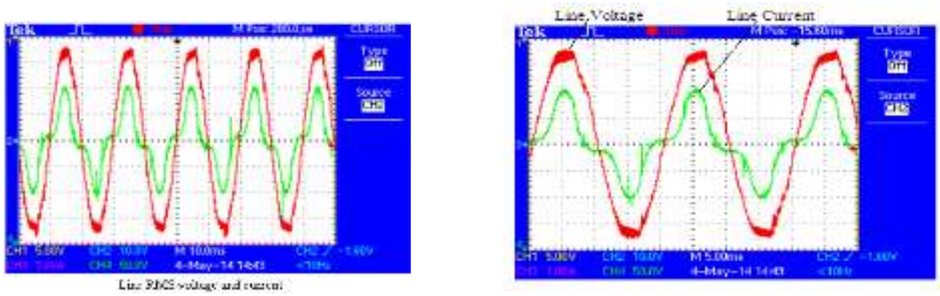


Fig. 6 Discarded 3rd harmonics and 5th and 7th harmonics reduction in Line current

4.2.1 Experiment Results to indicate PF in Rectification using CSPWM

The waveforms of the experiment results for the rectifying mode for various loads are presented in Fig. 7. The line current and voltage waveforms in Fig. 7(a) indicates a 0.80 PF at full load. This gives a result that is identical to the simulated waveform.The channel 1 is set at 50V/Divwhile channel 3 is adjusted at 1Amp/Div. At 80% load, more disturbances are appeared in line current. The observed PF of rectifier is 0.789 shown in Fig. 7(b).

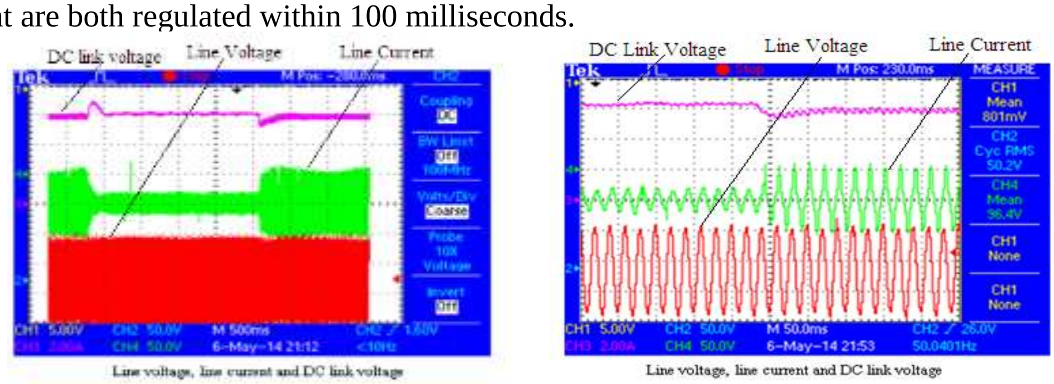


(a) (b)

Fig. 7 Experiment results (a) PF for full load condition, (b) PF for 80% load.

4.2.2 Experiment Results to indicate voltage regulation in Rectification using CSPWM

Fig. 8 illustrates the DC load is varied from 5% to 80% on a regular basis to determine output voltage regulation. The experiment result is shown in trace 'a' of Fig. 8, where it can be seen that as the load varies from 80% to 5% and then back to 80%, the DC link voltage regulation takes longer. Channels 2 and 4 are set to 50 volts per division, channel 3 is set to 2 amps per division, and the time/division knob is set to 500 milliseconds. The step variation and time of DC link voltage regulation after a load shift are visualized in trace 'b' of Fig. 8. It illustrates that after the load varies from 5% to 80%, the voltage and line current are both regulated within 100 milliseconds.



(a) (b)

Fig. 8 Experiment results of voltage regulations (a) DC load changes periodically load varies from 80% to 5% and 5% to 80%. (b)) DC load varies from 5% to 80% to show period of voltage regulation.

4.2.3 Experiment Result to show Bi-Directional operation

The CASE – II experimental results shows bi-directional operation, are same as of results of CASE - I. Same technique SPWM is applied for the inversion process in both cases. It shows the bi-directional operation of converter.

4.2.4 Line Current harmonic pattern

The harmonics pattern of line current is shown in Fig. 9. It is observed that 3rd, 5th and 7th harmonics are exists that boosts THD.

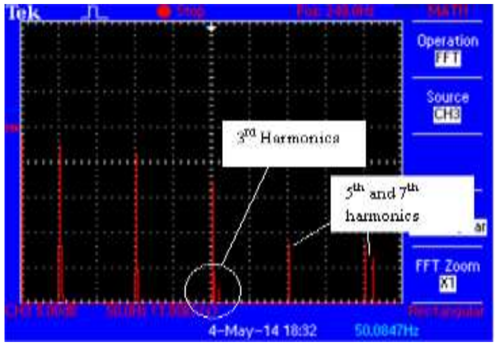


Fig. 9 Third, Fifth and seventh line current harmonics pattern

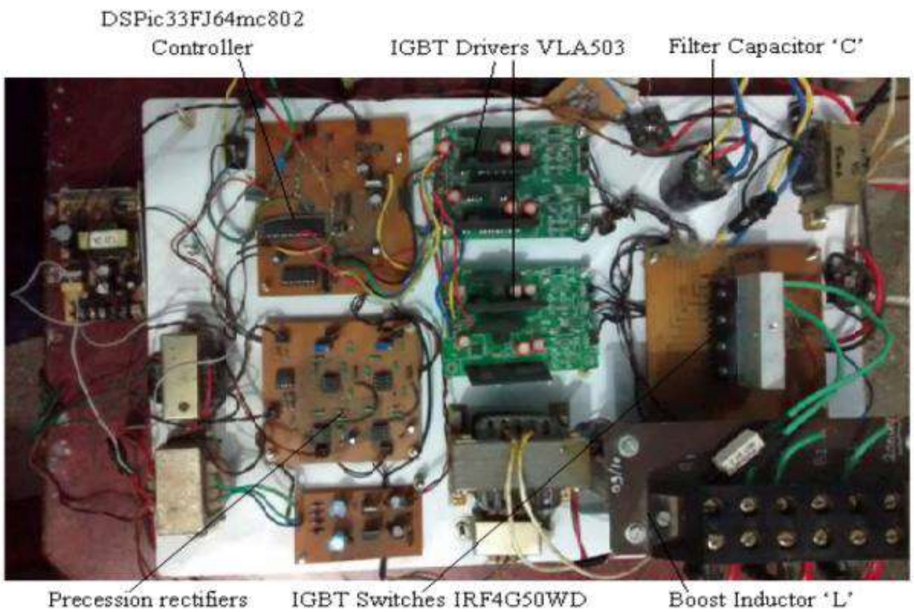


Fig. 10 Experimental Set-Up Of Laboratory Model

5. CONCLUSION

This paper presented Bi-Directional CSPWM and SPWM Converter with Improved PF and Harmonic Reduction Technique using two cases. It is shown that scheme using CASE – I exhibits remarkable results in terms of parameters like PF, voltage regulations, current harmonics and THD's compare to scheme with CASE – II. The result shows that full load efficiency and PF of 95.2% and 97.8% respectively for the CASE – I and for the CASE – II full load efficiency is 75.4% and PF is 80.3%. The voltage regulation period in first case is 40msec only and it is 100msec for the second case. The line current harmonics pattern yields better result for the case-I, the third harmonics are fully suppressed while fifth and seventh harmonics are suppressed up-to insignificant level. In case-II, the harmonics pattern of line current contains third, fifth and seventhharmonics that shows poor system performance. The converter system using case-I seems to be more advantages than system using case-II.

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