DESIGN ASPECTS OF ZVS FULL BRIDGE TOPOLOGIES

Dr. AJAYA KUMAR SWAIN,NIT,BBSR ajaykumar@thenalanda.com,

Mrs.SUBHASMITA CHAUDHURY,NIT,BBSR, subhasmita@thenalanda.com

Abstract:

As the load current decreases, the energy provided by the auxiliary circuit must increase to maintain ZVS, with the maximum energy required at no load. In this paper, a FB ZVS converter with adaptive energy storage that offers ZVS of the primary switches over a wide input voltage and load ranges with greatly reduced no-load circulating energy and with significantly reduced secondary side duty cycle loss is introduced. The proposed converter can be controlled by either constant-frequency phase-shift control or conventional PWM control.

Keywords: FB ZVS converter, snubber capacitor, of ZVS resonant converters

Introduction:

ZERO VOLTAGE SWITCHING RESONANT CONVERTERS

The switches of ZVS resonant converters turn on and off at zero voltage.

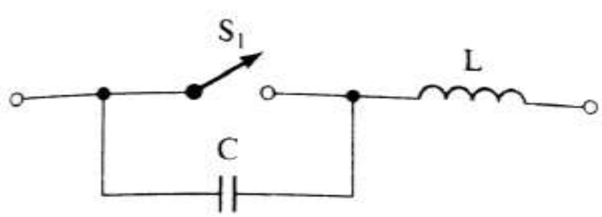

Fig. 1 ZVS CIRCUIT

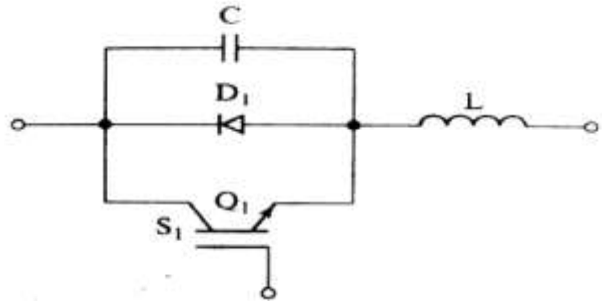

Fig. 2HALF WAVE

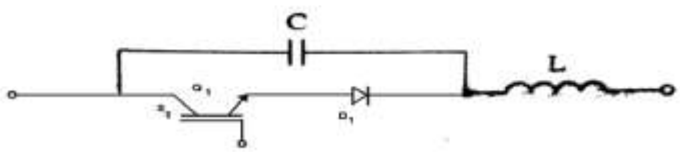

Fig.3 FULL WAVE

(Switch Configurations for ZVS Resonant Converters)

The capacitor **C_1** is connected in parallel with the switch **S_1** to achieve ZVS. The internal switch capacitance **C_1** is added with the capacitor **C** and it affects the resonant frequency only, thereby contributing no power dissipation in the switch. If the switch is implemented with transistor and an anti-parallel diode as shown in Fig.2.1., the voltage across **C** is clamped by the diode and the switch is operated in half wave configuration. If the diode **D1** is connected in series with **Q1** as shown in Fig.2.3, the voltage across **C** can oscillate freely and the switch is operated in full wave configuration. A ZVS resonant converter is shown. A ZVS resonant converter is the dual of ZCS resonant converter.

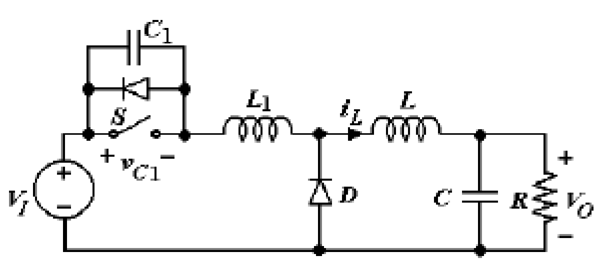

Fig. 4 ZVS Resonant Switch DC-DC Converter

To increase the switching frequency in DC-DC converters, and to reduce the electromagnetic interference produced due to high d*i*/d*t* and d*v*/d*t*, several modifications were made in conventional PWM (Pulse- Width-Modulation) converters.

The closed-loop control of the DC/DC converter prevents voltage variation, along with the variations due to the losses in the DC/DC converter itself, from appearing on the output DC bus. While the control "structure" for the PFC boost converter is necessitated by the need for power factor correction, the control concept utilized by the full-bridge DC/DC converter requires passing the output voltage control signal across the isolation boundary and then providing the necessary logic functions to pulse-width-modulate the four bridge switches based on this control signal. A much simpler method, at least conceptually, is to accomplish the necessary closed-loop regulation of the bus voltage entirely on the secondary. Here secondary-side switches modulate the volt seconds to the output inductor, thereby maintaining bus regulation without crossing the isolation barrier. The bridge switches on the primary can now be switched with a constant duty cycle, greatly simplifying the overall control scheme.

2. ZVS Full Bridge Topologies

Fig. 5 shows two typical full bridge topologies that achieve ZVS with passive components. In Fig, 6 ZVS is achieved by placing an inductor in series with the power transformer, while in Fig. 7 it is achieved by placing an inductor in parallel with the power transformer. In both topologies, a snubber capacitor is placed across each switch. In a practical configuration, the series inductor may be the leakage inductor of the power transformer, the parallel inductor may be the magnetizing inductor of the power transformer, and the snubber capacitor may be the inherent drain-to-source capacitor of the MOSFET switch. Addition of only one component to the full bridge converter makes these topologies the simplest. Several new techniques for high frequency DC-DC conversion have been proposed to reduce component stresses and switching losses while achieving high power density and improved performance. Among them, the phase-shifted zero-voltage-switching (ZVS) full bridge is one of the most attractive techniques since it allows all switches to operate at ZVS by utilizing transformer leakage inductance and metal oxide semiconductor field effect transistors (MOSFETs) junction capacitance without adding an auxiliary switch.

Moreover, based on the DCS PWM control, a new half-bridge topology is proposed to achieve ZVS for the other switch and auxiliary switch by adding an auxiliary switch and diode in the conventional half bridge. ZVS for the other switch is achieved by utilizing the energy trapped in the leakage inductance. In additional, the proposed topology with DCS PWM control eliminates the ringing result from the oscillation between the transformer leakage inductance and the switches junction capacitances during the off-time period. Therefore, the proposed converter has a potential to operate at higher efficiencies and switching frequencies.

(i) ZVS turn-off is achieved by holding the drain-to-source voltage of the MOSFET at zero or very low during the turn off transient. This is accomplished by the snubber capacitor. At turn-off, the snubber capacitor significantly slows down the rate of rise of the drain to source voltage of the pertinent switch. In this way, the overlap between the decreasing drain current and rising drain-to-source voltage of each switch is greatly reduced, or even completely eliminated, and so are the switching losses.

(ii) ZVS turn-on is achieved by completely discharging the snubber capacitors of the switches before they are turned on. During the dead time of the gating of the bridge switches, the discharging of the snubber capacitors is made possible by the residual current in the series inductor in the topology of Fig. 2.6, or the parallel inductor in the topology of Fig.2.7.

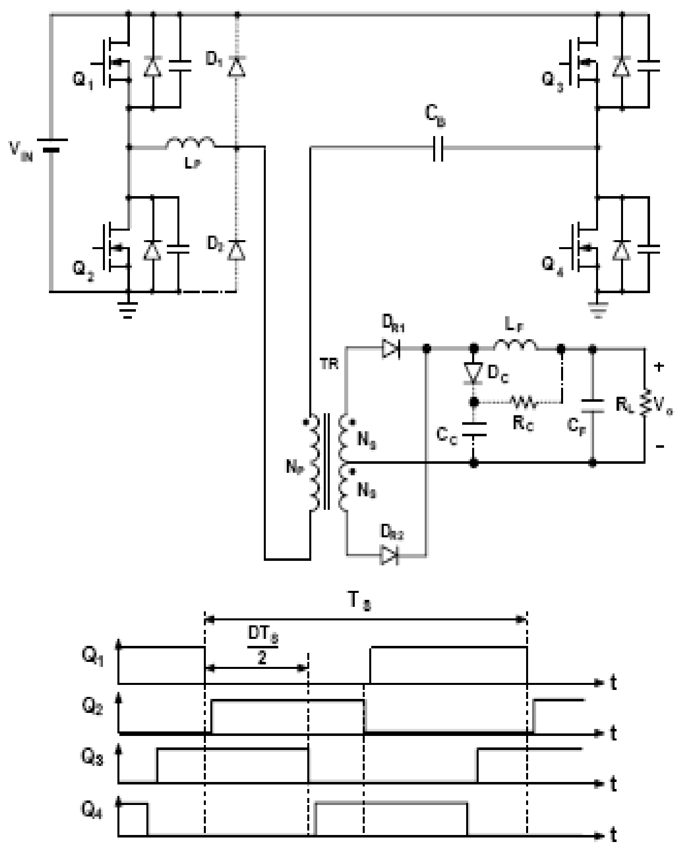

Fig 5 Conventional phase Shifted Full Bridge Converter and its Switch Timing Waveform

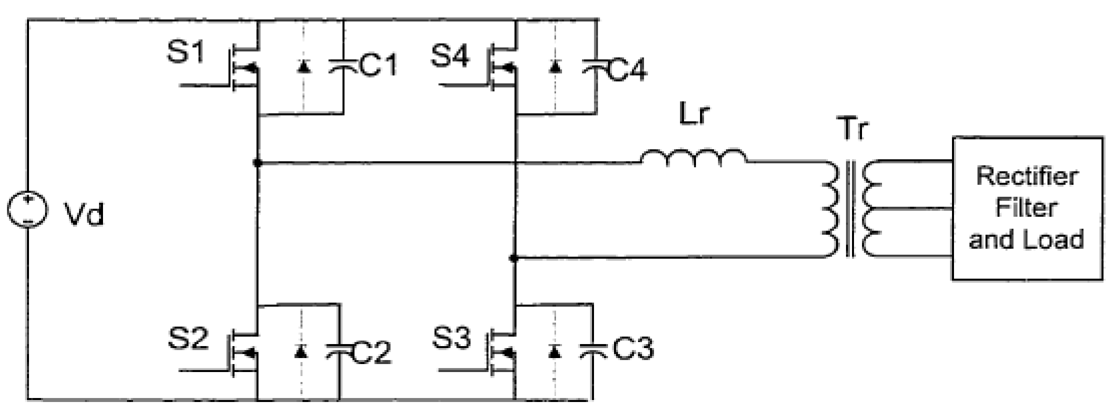

Fig.6.ZVS topology with series inductor

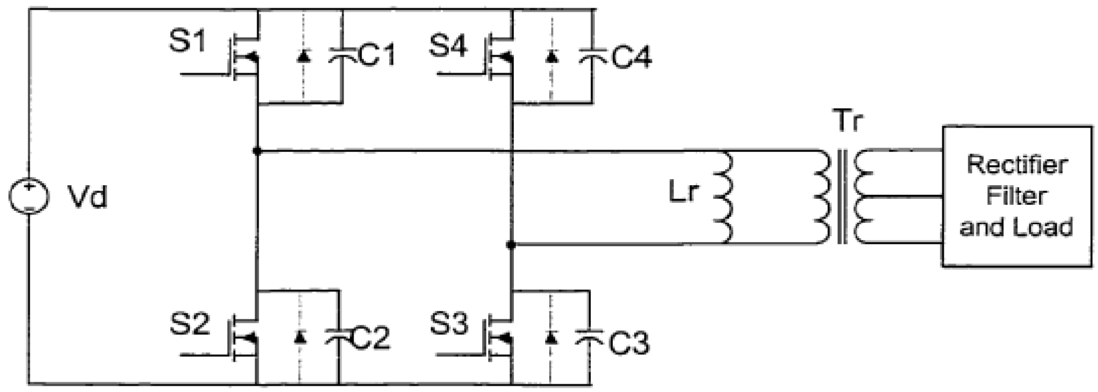

Fig.7.ZVS topology with parallel inductor

In comparison of these two topologies in Fig. 2.6 and 2.7, the one with the series inductor can achieve ZVS even when there is a short circuit (or over loading) across the load, while the other one that has the paralle1 inductor maintains ZVS operation even when there is an open circuit (or no load) across the output terminals. Both topologies are simple. However, both of them suffer from their own shortcomings

3. Drawbacks of topology

3.1With series inductor

Loss of ZVS at no load or light-load occurs in this case. This is because the complete discharge of snubber capacitors depends on the stored energy in inductor *L*, and the energy is proportional to the square of the peak value of the primary current, When the load is light, the primary current is low, and consequently the stored inductor energy is also low. This energy is not sufficient to deplete the snubber capacitor in the dead time. Thus, ZVS is lost at on. Reduction of the effective duty ratio because of the voltage drop on the series inductor. This results in higher primary current and conduction losses of the switches. ZVS topology with series inductor is shown in Fig 2.6.

3.2 With parallel inductor

ZVS topology with parallel inductor is shown in Fig 2.7. Loss of ZVS under over load or short-circuit conditions occurs in this case.. This is because, when the output terminals have a short circuit, the large load current, when it is reflected into the primary side, overrides the parallel inductor current and cancel its function to achieve ZVS. Increased conduction losses and reduced efficiency at light load. This is because the circulating current flowing along the parallel inductor, switch and the input dc Line is almost independent of the load level. At light load, the circulating current becomes significant compared to the load current, and this remarkably increases the total conduction losses at light load. It is seen that, both topologies lose ZVS under certain operating conditions. The loss of ZVS results in the following problems:

(i) increased size of heat sink due to switching losses,

(ii) higher EMI due to high di/dt of the snubber discharging current when the switch is turned on.

(iii) reduced reliability due to reverse recovery current of the body diodes.

4. Soft Switching Full Bridge Topologies (Active Mechanism)

Fig. 8 shows a soft switching full bridge topology with active components. It employs two symmetrical auxiliary circuits, each of which is controlled through an auxiliary bidirectional switch. In order to control the current through the auxiliary inductors, each bidirectional switch must be implemented by using two anti-paralleled unidirectional switches. By proper timing, the current building up in the auxiliary inductor discharges the Snubber capacitor the pertinent switch to achieve its ZVS turn-on, or overcomes the tail current of the pertinent switch to achieve ZCS turn-off. Soft switching can be achieved under all operating conditions, thereby overcoming the aforementioned drawbacks existing in the topologies show in Fig6 and 7.

Specifically, it achieves soft switching even under bath extreme operating conditions, namely no load and output short circuit conditions, and there is no reduction of the effective duty ratio.

The topology in Fig. 8 is originally developed for high power full-bridge converters using IGBTs. For lower power level applications, when MOSFETs are used, the topology of Fig. 8 is directly converted into Fig. 9.

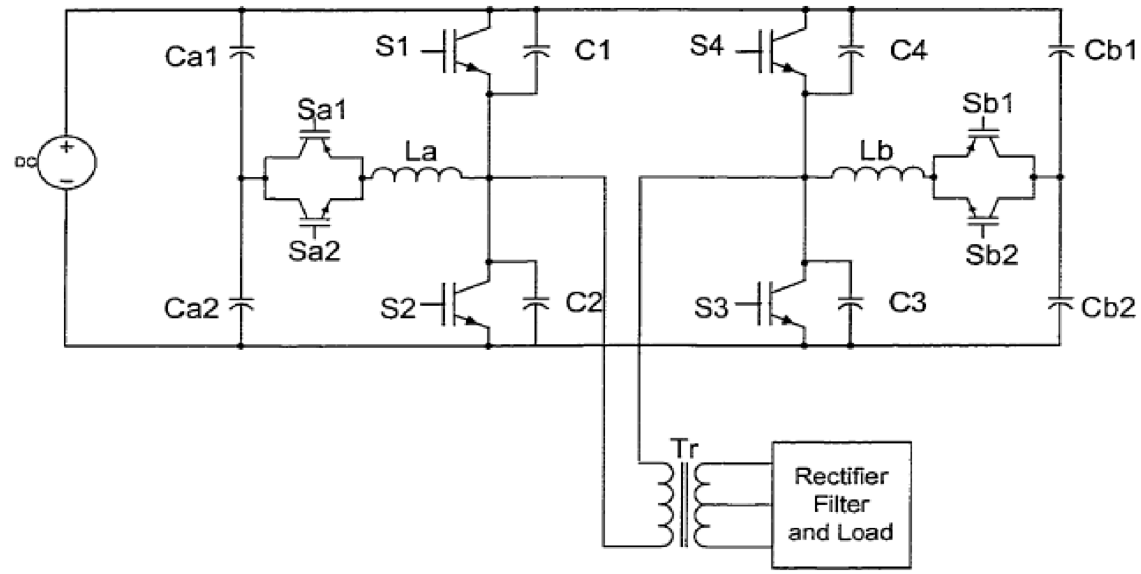

Fig. 8. Soft switching Full bridge converter IGBT topology using active auxiliary switch.

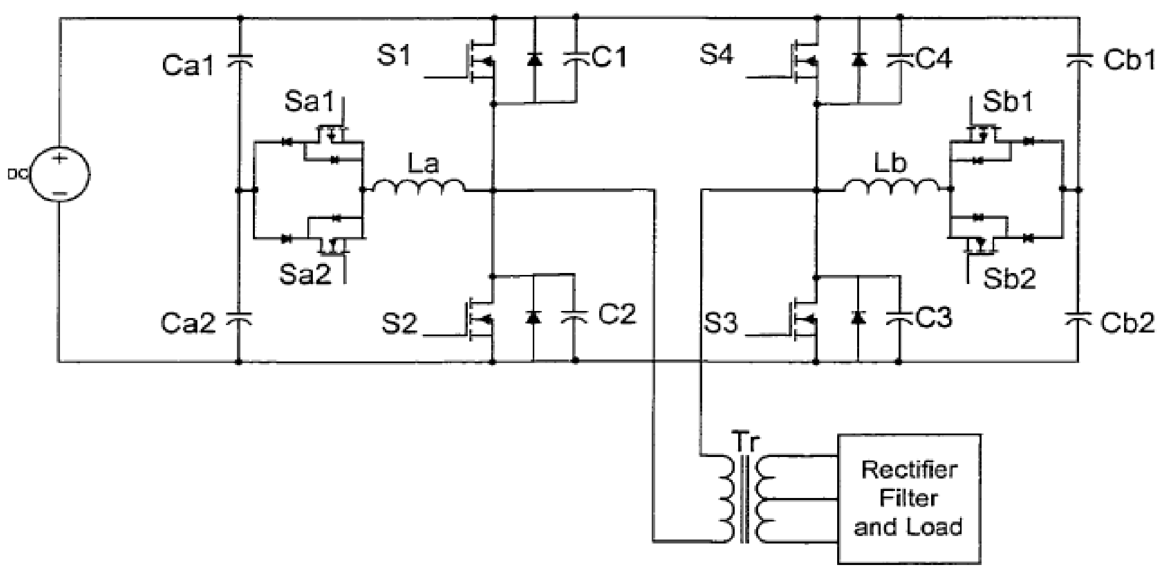

Fig. 9 Soft switching Full bridge converter MOSFET topology using active auxiliary switch Based

As seen from Fig. 2.9, each unidirectional switch in the auxiliary circuit requires an additional fast speed diode in series with a MOSFET, The topology becomes rather complicated and costly for low power level applications- Simplified ZVS topologies shall be developed to overcome these problems.

5. CONCLUSION:

As the load current decreases, the energy provided by the auxiliary circuit must increase to maintain ZVS, with the maximum energy required at no load. In this paper, a FB ZVS converter with adaptive energy storage that offers ZVS of the primary switches over a wide input voltage and load ranges with greatly reduced no-load circulating energy and with significantly reduced secondary side duty cycle loss is introduced. The proposed converter can be controlled by either constant-frequency phase-shift control or conventional PWM control.

References:

[1]. N.G. Hingorani, L. Gyugyi, "*Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems," IEEE Press*, N.Y., 2000.

[2]. Y.H. Song, A.T. Johns, "*Flexible AC Transmission Systems – FACTS," IEE Press*, London, UK, 1999.

[3]. K. R. Padiyar, "FACTS Controllers in Power Transmission and Distribution", *New Age International (P) Limited Publishers* (formerly Wiley Eastern Limited), 2007, New Delhi.

[4]. H.Saadat," Power System Analysis," *Tata McGraw-Hill* Edition, 2002.

[5]. P. Kundur, "Power System Stability and control", *New York, McGraw-Hill*, 1994

[6]. R.L.V. Arnez, L.C. Zanetta Jr., "48-Pulse Based SSSC (Static Synchronous Series Compensator) an Evaluation of its Performance," in Proc. WSEAS *International Conferences on: System Science, Applied Mathematics & Computer Science and Power Engineering Systems 2002*, Rio de Janeiro, Brazil, Oct. 21-24, 2002.

[7]. M. Noroozian, L. Angquist, and G. Ingestrom, "Series compensation," in *Flexible ac Transmission Systems (FACTS)*, Y. H. Song and A. T. Johns, Eds. London, U.K.: *IEE, 1999*, pp. 199–242.

[8]. R. Billinton, M. Fotuhi-Firuzabad, and S. O. Faried, "Power system reliability enhancement using a thyristor controlled series capacitor," *IEEE Trans. Power Syst*., vol. 14, no. 1, pp. 369–374, Feb. 1999.

[9]. K. R. Padiyar, Nagesh Prabhu, "Analysis of SSR With Three Level Twelve Pulse VSC Based Interline Power Flow Controller", IEEE Transactions on Power Delivery, Vol.20, No.3, July 2007.

[10]. K. R. Padiyar, N.Prabhu, "Analysis of Subsynchronous Resonance with Three level Twelve Pulse VSC Based SSSC", Proceedings of IEEE TENCON, Oct. 14 – 17, 2003, pp. 76 – 80.

[11]. K. R. Padiyar, N. Prabhu, " Modelling, Control Design and Analysis of VSC Based HVDC Transmission Systems", presented at the IEEE POWERCON, Singapore, Nov.21 – 24, 2004.

[12]. Taha Selim, Saad Mekhilef, "Power Line Compensation Study of a Static Synchronous Series Compensator (SSSC) Based on Soft Switching 48 Pulse PWM Inverter", Australian Journal of Basic and Applied Sciences, 3(2), 1301 – 1314, 2009.

[13]. R. Billinton, M. Fotuhi-Firuzabad, and S. O. Faried, "Sub Transmission system reliability enhancement using a thyristor controlled series capacitor," *IEEE Trans. Power Del.*, vol. 15, no. 1, pp. 443–449, Jan. 2000.

[14]. U. Gabrijel and R. Mihalic, "Direct methods for transient stability assessment in power systems comprising controllable series devices," *IEEE Trans. Power Syst.*, vol. 17, no. 4, pp. 1116–1122, Nov. 2002.

