Fin-FET based Energy efficient and density aware parallel to serial block using multiplexer

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ABSTRACT: FinFET, which is a double-gate field effect transistor (DGFET), is more versatile than traditional single-gate field effect transistors because it has two gates that can be controlled independently. Usually, the second gate of FinFETs is used to dynamically control the threshold voltage of the first gate in order to improve circuit performance and reduce leakage power. However, this concept also utilize the second gate to implement circuits with fewer transistors. The backend device Tanner EDA is selected for the analysis of power dissipation and put off of multiplexer along with decoder. In this paper, 7- enter multiplexers are designed and simulated in 7 nm era the usage of FinFET technology. Simulation end result imply that the proposed technique offer improvement in term of strength consumption and delay over MOSFET. This research introduces another need for higher performance applications with low power consumption as we see there is lots of difficulty in using low power devices for a higher rank application like microprocessor, DSP, SRAM. As we know the Decoder plays an important role in memory design & logical circuit design.

Keywords: Fin-FET, Complementary Metal Oxide, double-gate field effect transistor, multiplexer, Parallel to serial transmission.

INTRODUCTION: Static CMOS circuits are utilized for most by far of logic gates in incorporated circuits. [1]They comprise of correlative nMOS pull down and pMOS pull up systems and present great execution just as protection from commotion and gadget variety. In this way, CMOS logic is described by power against voltage scaling and transistor estimating and accordingly dependable task at low voltages and little transistor sizes. [2] Information signals are associated with transistor gates just, offering decreased plan unpredictability and assistance of cell-based logic blend and structure. Pass transistor logic was primarily created during the 1990s, when different structure styles were presented, planning to give a feasible option to CMOS logic and improve speed, power and zone. [3][4] Its primary plan distinction is that inputs are connected to both the gates and the source/drain dispersion terminals of transistors. Pass transistor circuits are actualized with either individual nMOS/pMOS pass transistors or parallel sets of nMOS and pMOS called transmission gates. This work builds up a mixed-logic plan approach for line decoders, joining gates of various logic to a similar circuit, with an end goal to get improved execution contrasted with single-style structure. [5] Line decoders are major circuits, generally utilized in the fringe hardware of memory exhibits (for example SRAM), multiplexing structures, usage of Boolean logic capacities and different applications. Regardless of their significance, a generally little measure of writing is devoted to their streamlining, with some ongoing work including and a method to propose a better technique is presented. [6][11]. This task investigates how circuits dependent on FinFET, a developing transistor technology that is probably going to enhance or displace mass CMOS (C metal-oxide- semiconductor) at 22-

nm and past, offer intriguing delay– power trade offs. Since the origins of the IC company, the desire to strengthen the structural measurements of performance, energy, area, price and time to advertise has not altered. It is true that the law of Moore is linked to the progress of these parameters. In any event as the mounting jacks increased to 20-nm, a portion of the gadget parameters could not be further scaled to the variable prevailing in the definition of a unique power supply, particularly the power supply voltage. Moreover, for instance, upgrading one factor has transformed execution into huge trade-offs in various regions, comparable to power. The lithography was attached to Arm's brightening source with a 193 nm wavelength, while the procedure basic element pushed sub-20 nm, another restriction when procedures rose to 20nm. For example, optical advances in drenching lithography and dual adjustment made that conceivable; but, at the expense of increased variation.

LITERATURE SURVEY: A mixed-logic line decoder framework consisting of door transmission logic, double-estate transistor logic and static CMOS was reported [1]. The 2-4 decoders display two story topologies: a topology with a 14-transistor pointing to limit the number of transistors and dispersion of energy and a topology of 15-transistors showing elevated energy deferment. The review [2] incorporates a few distinct perspectives, for example, circuit advancements, structure and amalgamation philosophies, applications and business use, and so forth. The circuit advancements and amalgamation strategies are generally assembled into two classes, one of which has a nearby connection to BDD, while different does not. Circuit advances are likewise classified into various tomahawks, For instance, differential or single-rail structure, NMOS or CMOS, static or dynamic circuit, and so forth. Along with these tomahawks classification, the highlights of each pass transistor logic family are explained. A study covers the two of these, the decoder and the multiplexer [3]. In this reported study, planning of 2:1 MUX and MUX Based Decoder utilizing SCL (Source Coupled Logic) is done. Power and estimation of current spike (Rail– to-Rail current) is found for the circuits. The Simulation is done utilizing 180 nm technology utilizing TANNER (Version 9.2) apparatus. A philosophy dependent on unate deterioration to understand a mixed static Domino circuit has been proposed [4]. A calculation for breaking down a Boolean circuit into unate and binate sub squares has been presented. Utilizing an influence table methodology, the deterioration calculation gets the most extreme unate set, containing states that can understand a Domino square. GDI process reduces energy, delays in proliferation, amount of transistors, maintaining the low complexity of the constructions [5]. All proposed decoders are planned in Gate dissemination input (GDI)—another procedure of lowpower computerized combinatorial circuit configuration in this manner brings about lessening power utilization, proliferation deferral, and territory of advanced circuits while keeping up the low multifaceted nature of the logic structure. A selection of 32 nm close-focus reproductions shows that a significant increase in power and postponement occurs in the suggested circuits, beating CMOS almost in all instances [6]. SRAMs are critical structure hinders in numerous computerized applications, for example, chip and reserve recollections [7]. Decoders are the huge segments in SRAMs. Address decoder is essential piece of SRAM memory. Decision of limit cell and read task depends upon decoder. From this time forward, execution of SRAM depends upon these parts. This work thinks about the area decoder for SRAM memory, concentrating on deferral streamlining and control successful circuit frameworks.

Fin-FET based Parallel to Serial implementation: Former TSMC CTO and Berkeley professor Chenming Hu and his team presented the concept of FinFET in 1999 and UTB-SOI (FD SOI) in 2000. The main principle behind both the structures is a thin body, so the gate capacitance is closer to whole channel. The body is very thin, around 10nm or less. So, there is no leakage path which is far from the gate. The gate can effectively control the leakage. The basic structure of FinFET which they proposed would be a channel controlled by more than one side of channel. One of the Double-Gate Structures is shown in Figure 1.

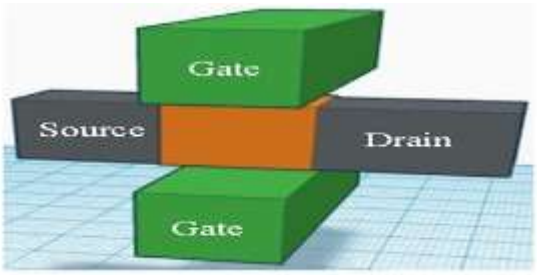

Figure 1. Double Gate Structure

Modern FinFETs are 3D structures as shown in the Figure 5.2 also called tri-gate transistor. FinFETs can be implemented either on bulk silicon or SOI wafer. This FinFET structure consists of thin (vertical) fin of silicon body on a substrate. The gate is wrapped around the channel providing excellent control from three sides of the channel. This structure is called the FinFET because its Si body resembles the back fin of a fish.

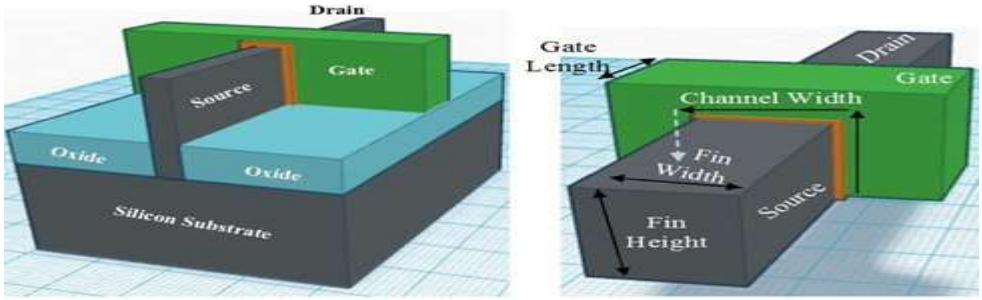

Figure 2. Fin-FET Structure

In bulk-MOS (planner MOS), the channel is horizontal. While in FinFET channel, it is vertical. So for FinFET, the height of the channel (Fin) determines the width of the device. The perfect width of the channel is given by Equation 4.

Width of Channel = 2 X Fin Height + Fin Width (Equation-4)
(Source: Synopsys)

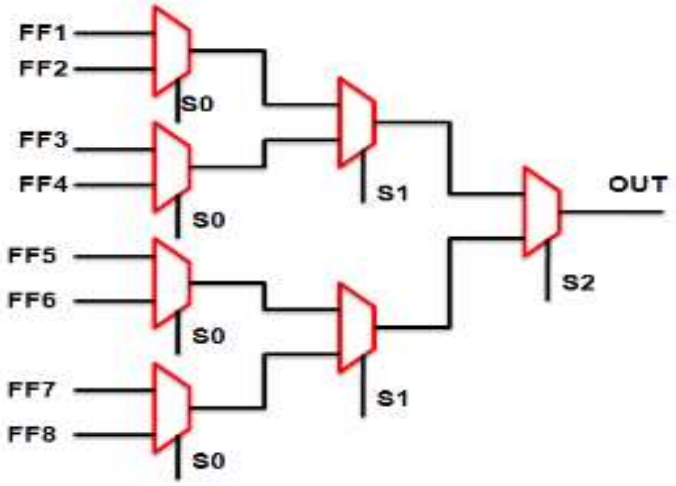

Fig3 Parallel to serial block using Fin-fet multiplexers

Total 8 FFs, each working at a frequency of 10MHz and sending out a parallel data which effectively would be 8-bit wide. We intend to convert this data into a serial one, where 1 FF would output the data serially in order of first FF, then data of second FF and so on. Refer to the diagram below:

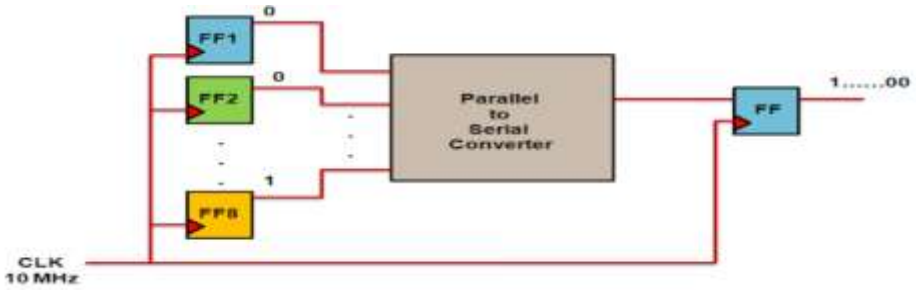

Fig4: Parallel to serial with control block

Such a parallel to serial converter might be useful in applications requiring Serial Communication which maybe interface to a microprocessor or a microcontroller; interface between your monitor and the CPU or any application which might involve serial processing of information.

Fin-FET based DFF for memory cell: Static RAM is a kind of RAM that holds data in static form until the memory has power. There is no need for periodic refreshing in SRAM. Since it is volatile, the data gets lost if it is not powered. SRAM makes use of bi-stable latching circuitry in order to store each bit. SRAM is used in internal CPU caches, workstations, PCs, and hard disk buffers etc. The structure of SRAM array includes the following: Bit line, Sense amplifier, Word line, Row and Column decoder and Storage cell. Numerous words are stored in a single row and are selected simultaneously. Address word is divided into a row and column addresses. To perform read or else write operation, only one row of memory is enabled by the row address whereas the column address selects one from the selected row. The storage cell is otherwise named as 1-bit memory cell or bit-cell which includes a latch circuit (2-cross coupled inverters) with dual main operating states. The data present in the storage cell can be represented as logic '1' or '0'. SRAM cell consists of 3 different operational states. Standby or Hold (Circuit is idle) Read (Request for

data) Write (contents updating) SRAM memory cell is normally be made of simple cross-coupled inverters that are connected back to back, and two access transistors [23]. Whenever a word line (WL) is activated for read or write operation, the access transistors are turned ON connecting the cell to the complementary bit line (BL) columns. Some advantages of this circuit topology are static power dissipation (SPD) is very small, medium power consumption, small leakage current, and need less time to access data.

Fin-Fet 9T SRAM:

The schematic of reported 9T SRAM cell is represented in Fig. 3 The Sub-18 nm high performance(HP) and low standby power(LSTP) FinFET predictive technology model (PTM) is used for 9T SRAM cell design and simulation. The proposed design is a well featured modified design of recently designed 8T SRAM cell [5]. The structural improvement of a bit cell is examined to enhance the stability of the cell in a near-threshold region and the bit cell robustness is optimum under the process, voltage and temperature variations. The proposed 9T SRAM bit cell has asymmetrical cross-connected inverter pair. The right face inverter comprises four FinFET transistors (M3-M4- M5-M6) and left face inverter comprises two FinFET transistors(M1–M2). To improve the write margin and write time of bit cell, low Vt (LVT) transmission gate is employed as an access transistor. Furthermore, dual threshold technique is implemented for high performance and low power applications simultaneously. The transistors M4, M5, M7, and M8 have 2 fins for higher drive strength and M1, M2, M3, M6, and M9 have 1 fin to reduce area overhead as shown in Table 1. High threshold transistor(HVT) and low threshold transistor(LVT) are also employed properly to achieve high performance and low power at the same time in proposed bit cell which is illustrated in Table 2.

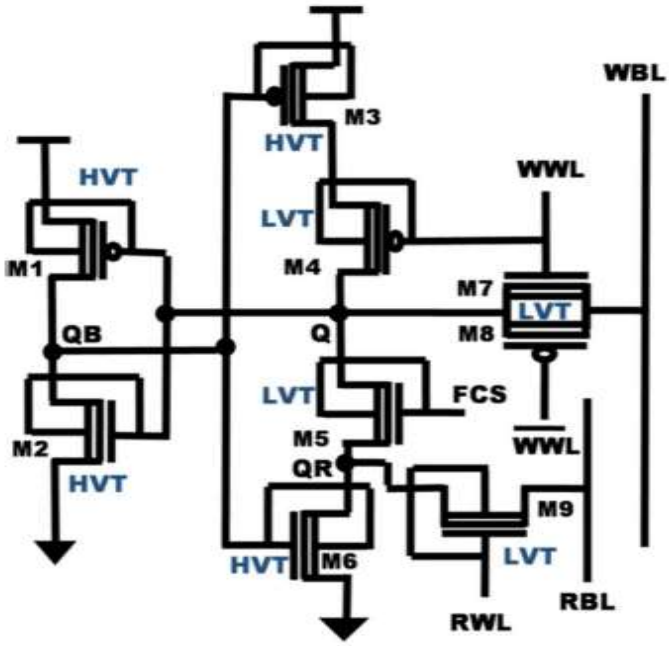

Fig5 Schematic of proposed 9T SRAM cell

Table 1 Transistor sizing of reported SRAM cells.

Bit- Cell Design	Access FinFET (No. of Fins)	Pull-up FinFET (No. of Fins)	Pull-down FinFET (No. of Fins)	Feedback Cutting FinFET (No. of Fins)	Read transistor (No. of Fins)
6T	M5=M6=1	M3=1, M4=1	M1=1, M2=1	-	-
7T	M4=1, M7=1	M3=1, M5=1	M1=1, M6=1	-	M2=1
8T	M7=2	M8=1, M1=1	M5=M4=1	M2=M6=2	M3=1
9T	M7=M8=2	M3=M1=1	M2=M6=1	M4=M5=2	M9=1

Fin-FET based 4:1 multiplexer:

Below shows the circuit diagram of 4:1 MUX using the proposed technique. Here, S0 and S1 are the select lines and A, B, C and D are the inputs to the MUX. The truth table of the MUX is as shown in below Table. The evaluation logic consists of four combinations in parallel. One of the four inputs is selected by the select lines S0 and S1.

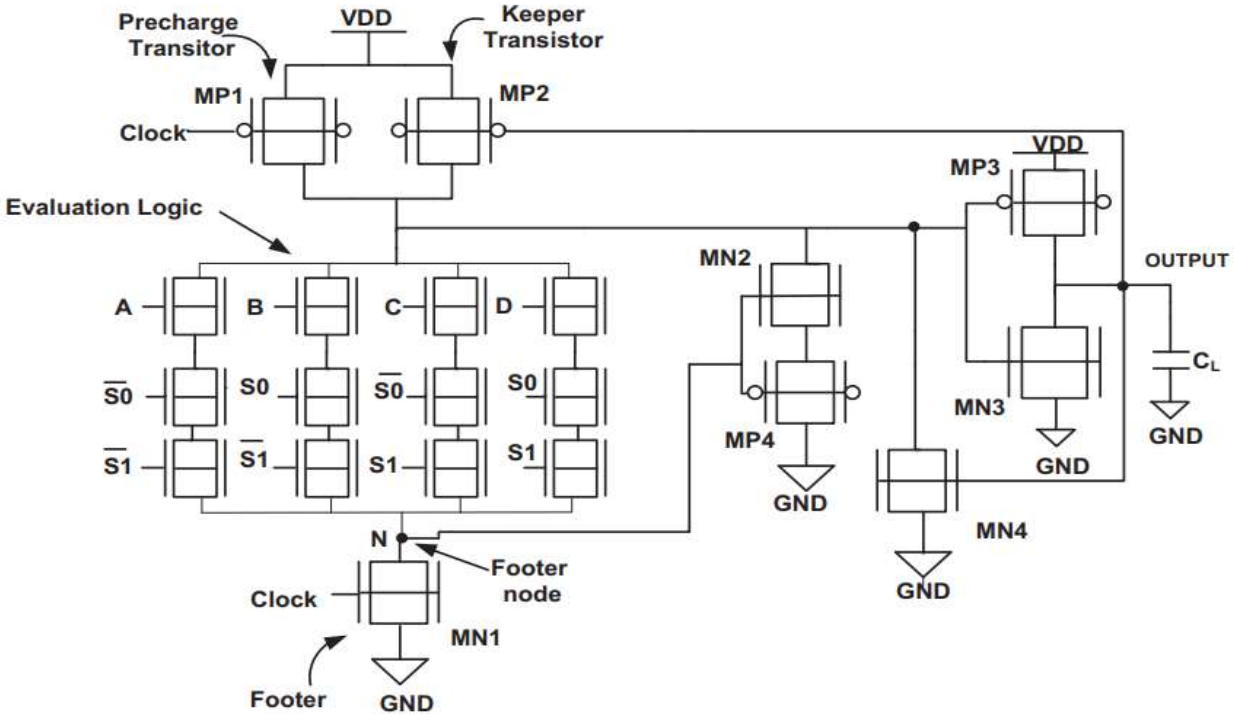

Figure 6 A 4:1 MUX (Multiplexer) using the proposed LPSC-FDTL technique in SG mode

Low power series connected foot-driven transistors logic (LPSC-FDTL) in SG mode:

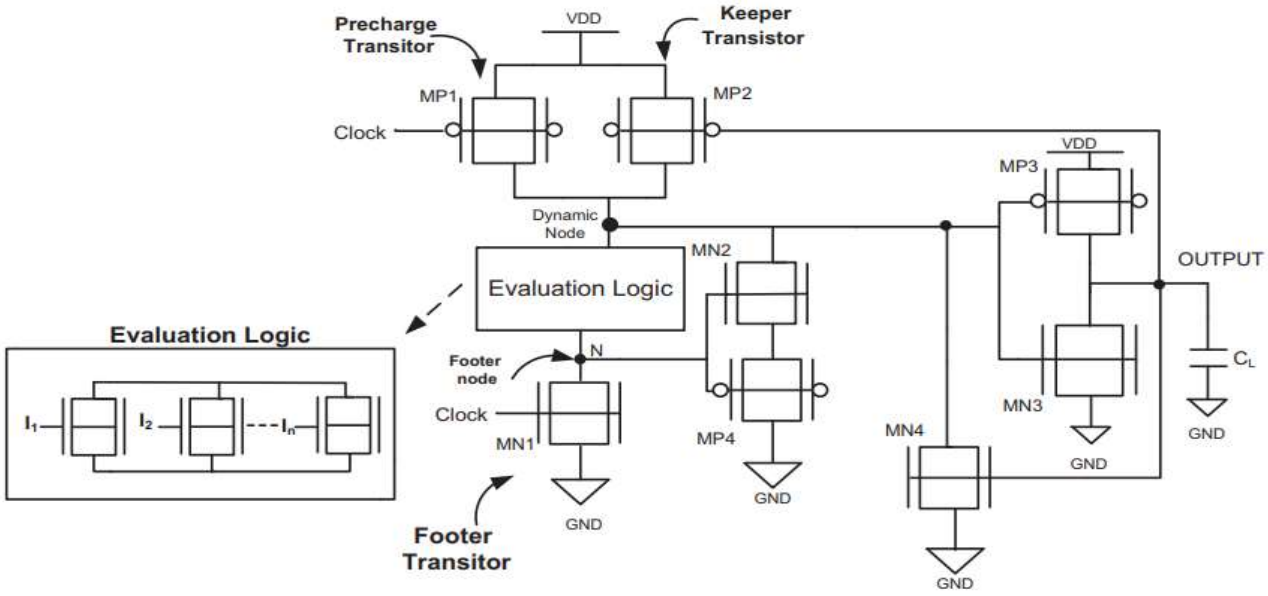

Fig:7 Proposed low power series connected foot-driven transistors logic (LPSC-FDTL) in SG mode

A new domino-style is proposed in this section for designing high fan-in gates. This technique is termed as low power series connected foot-driven transistors logic (LPSC-FDTL). The technique is simulated for two modes, SG mode and LP mode as shown in above figure. The circuit comprises of two sections, input sections have MP1 as a precharge transistor, evaluation logic having NMOS transistors in parallel (for OR gate) and MN1 as footer transistor, whereas the output section comprises of keeper transistor MP2, the static inverter comprises PMOS transistor MP3 and NMOS comprises transistor MN3 and transistors MP4, MN2 and MN4. The inputs to the circuit are applied at the gate of the NMOS transistors in the evaluation network. Transistors MP4 and MN2 are fed by the voltage at the footed node N as shown in Figure 5.8 Transistor MN4 is connected between the dynamic node and ground. Gate of MN4 is fed by the output voltage. MN4 acts as a feedback transistor. The proposed circuit uses stacking of transistors MN2 and MP4 that reduces leakage current between dynamic node and ground, thus reducing the leakage power consumption of the circuit. In addition, the proposed circuit has low transistor count that reduces the power consumption, propagation delay and area of the circuit in comparison with existing techniques. There are no additional inverter-delay elements in the proposed circuit that further enhances the speed of the circuit compared to existing techniques. The proposed technique has a higher noise margin or UNG in comparison with existing techniques because of the feedback transistor MN4 that prevents the undesirable discharge of dynamic node by providing feedback from the output.

RESULSTS

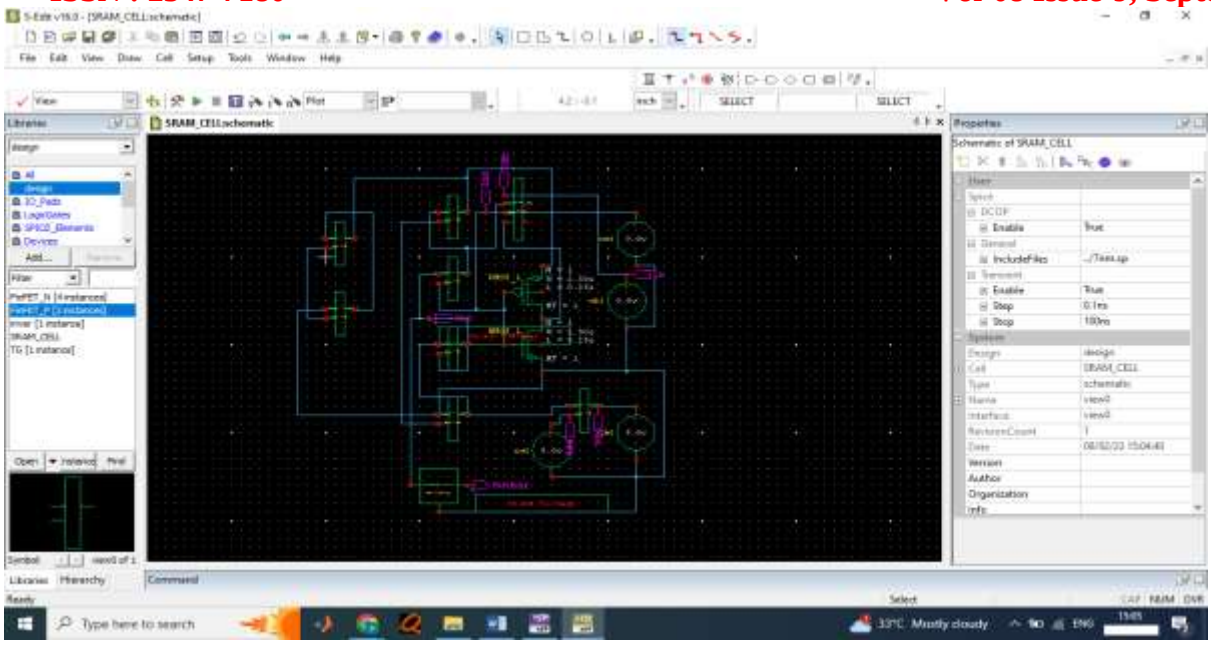

Fig8.1: Proposed SRAM design

Above screenshot taken in Tanner EDA16.0 represents proposed FinFET based SRAM design using 9T SRAM with 7nm technology.

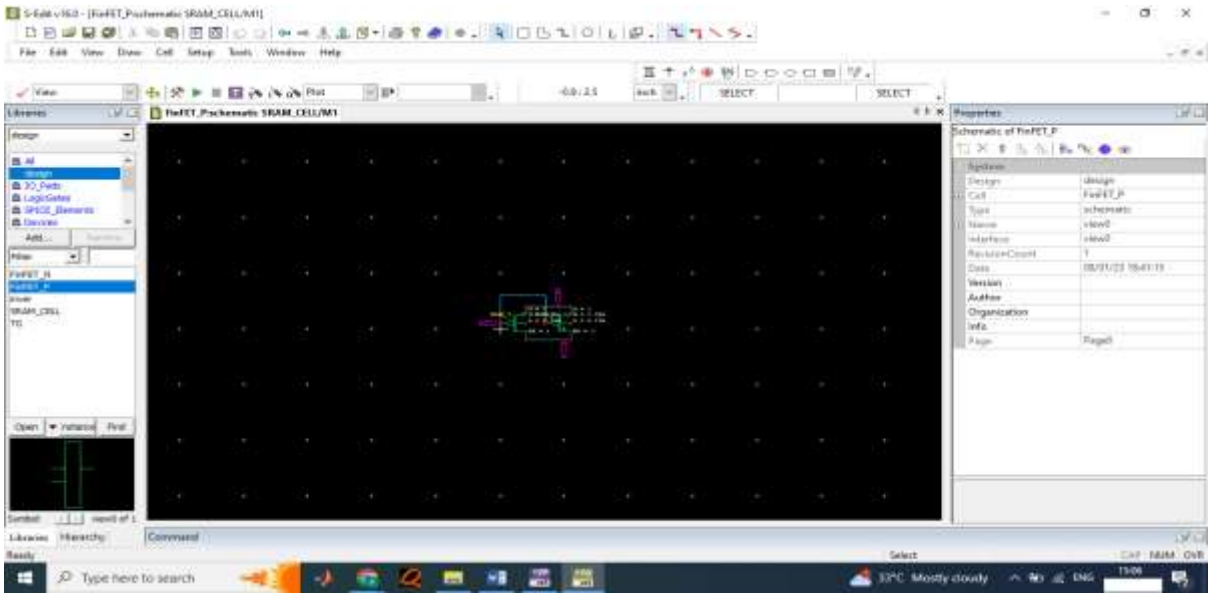

Fig8.2: Proposed FinFET design

Above figure shows FinFET internal architecture with two gate PMOS

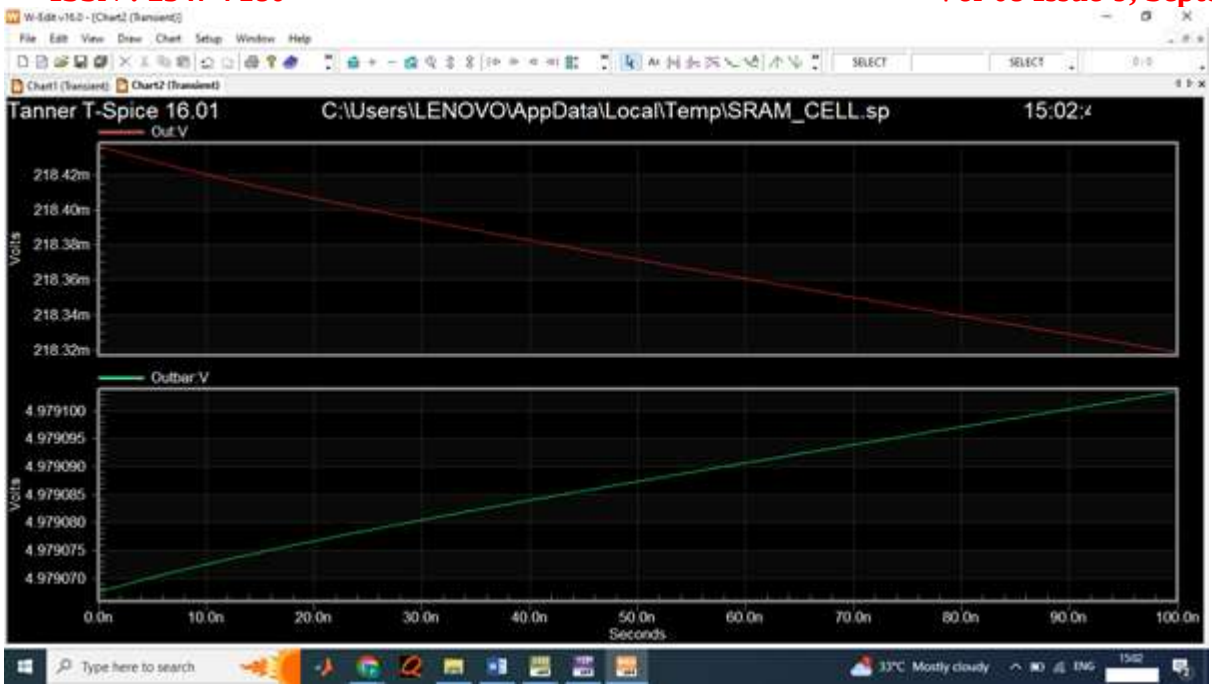

Fig8.3: Storing '0'

Above result shows proposed 9T SRAM '0' storing graph.

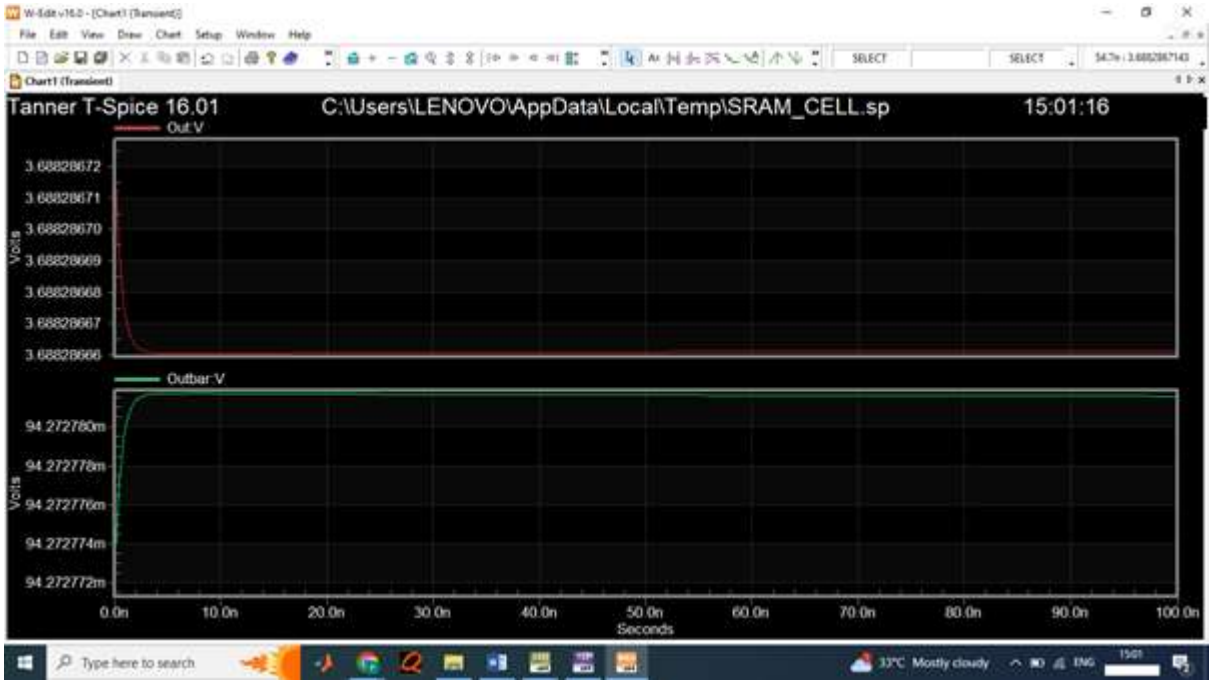

Fig8.4: Storing '1'

Above result shows proposed 9T SRAM '1' storing graph.

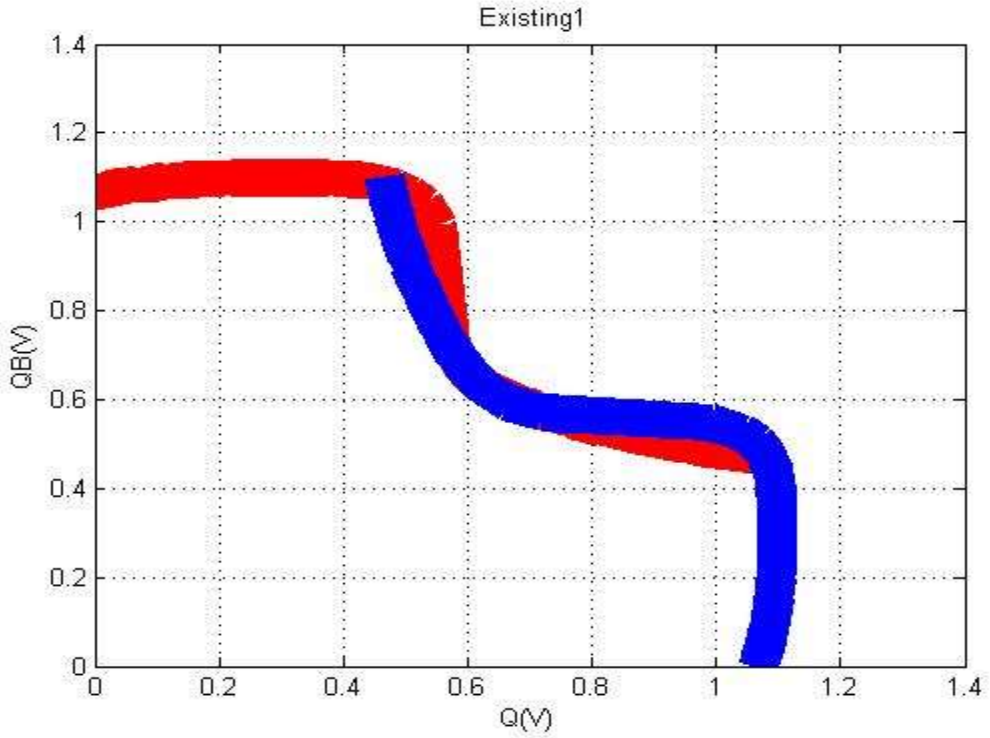

Fig8.5: SNM for Existing method1

Above Graph represents existing SNM with unstable write read performance.

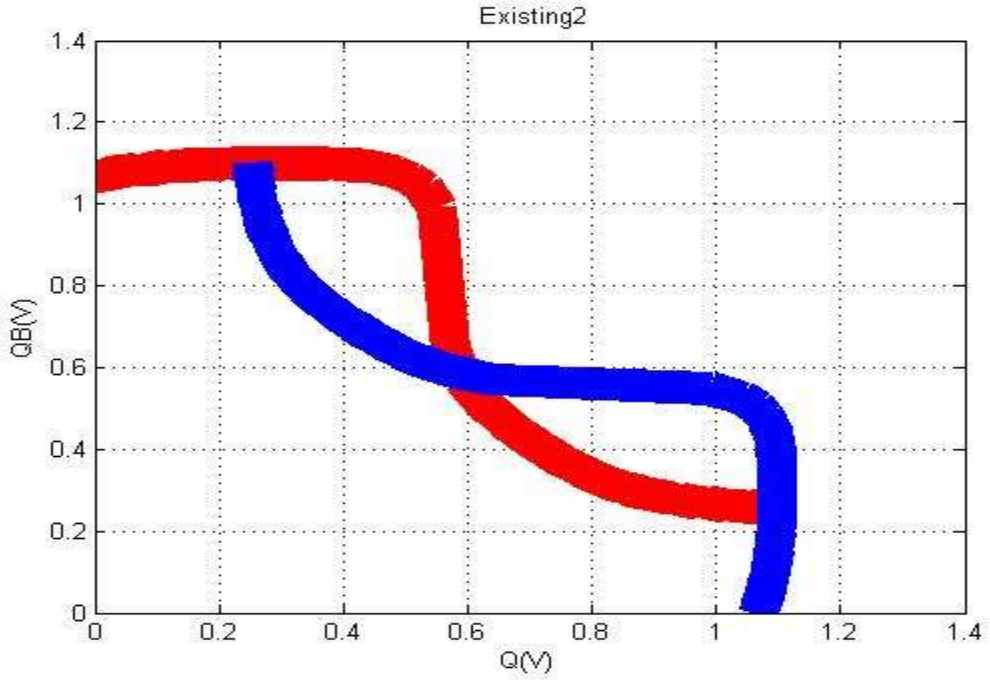

Fig8.6: SNM for Existing method2

Above Graph represents second existing SNM with unstable write read performance.

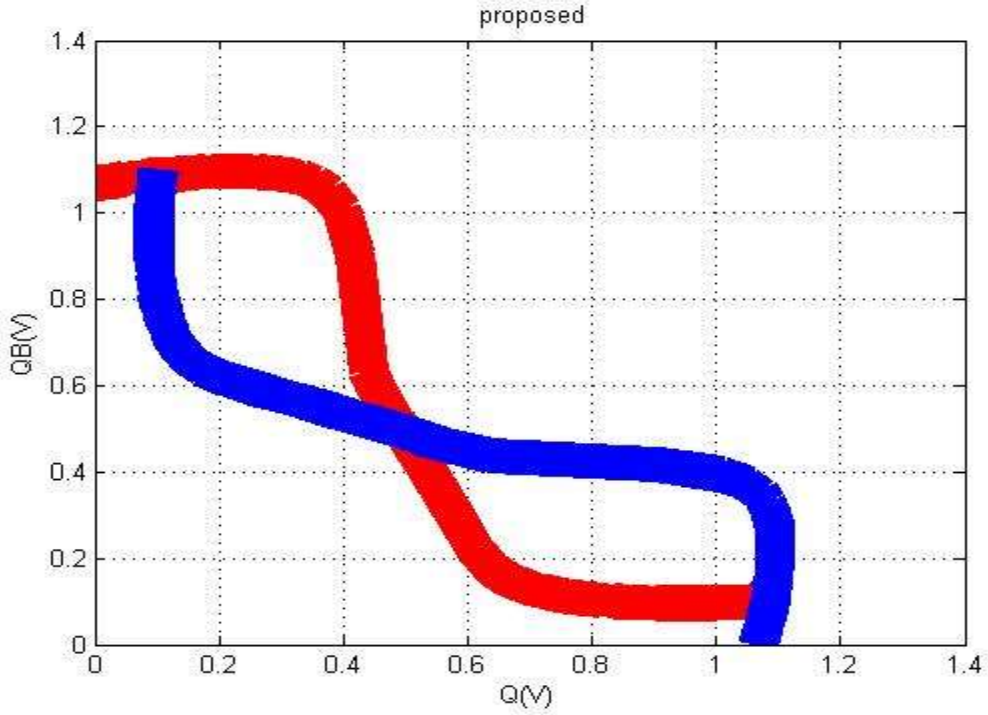

Fig8.7: SNM for Proposed method

Above Graph represents proposed SNM with stable write read performance.

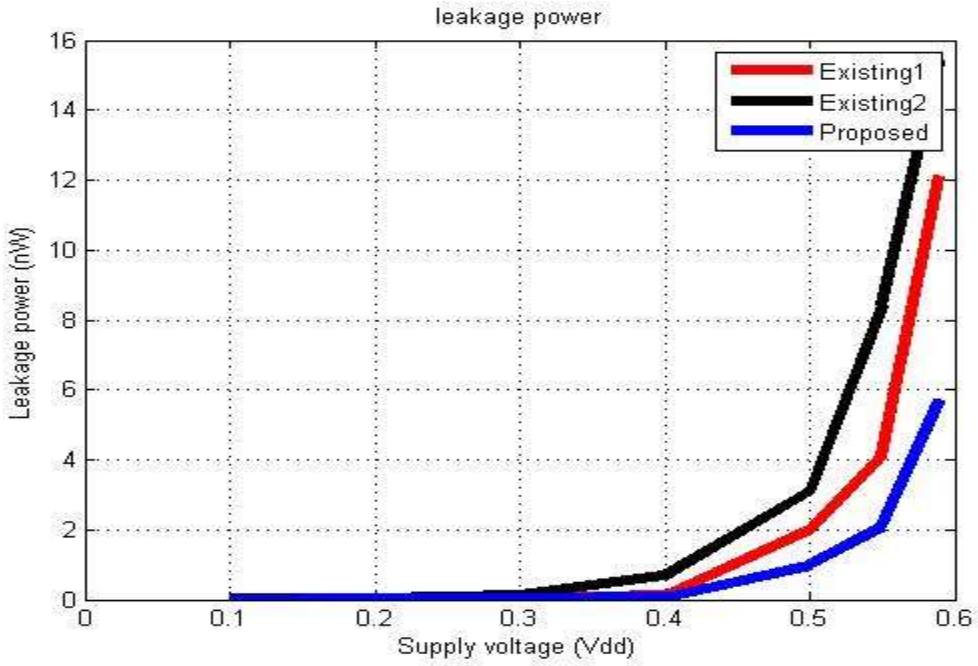

Fig8.8: Leakage power comparison

Above Graph represents leakage power comparison of proposed and existing methods

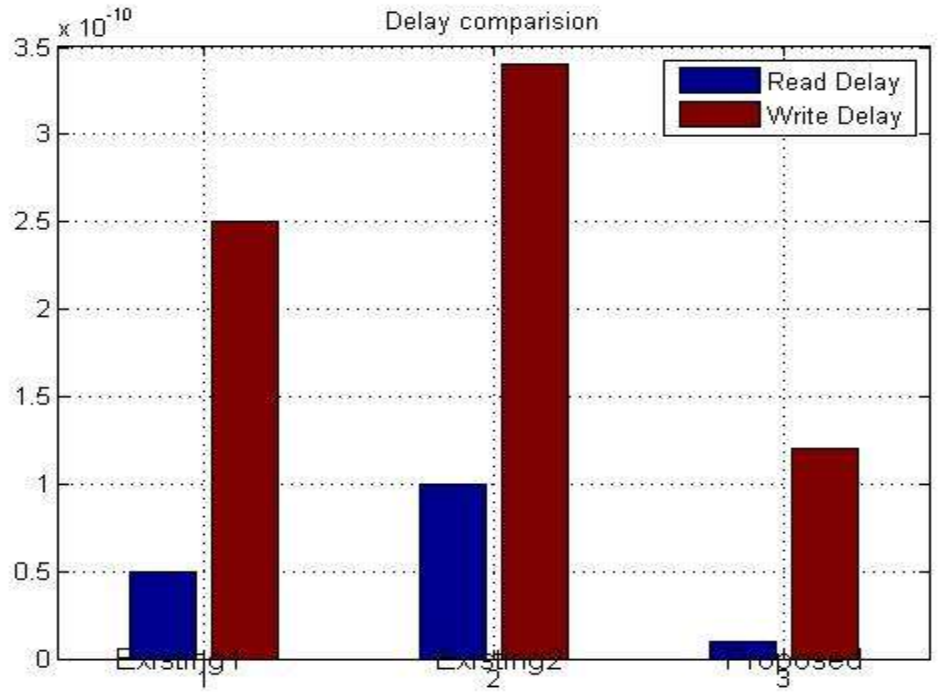

Fig8.9: Latency comparison

Above Graph represents whole execution time delay comparison of proposed and existing methods

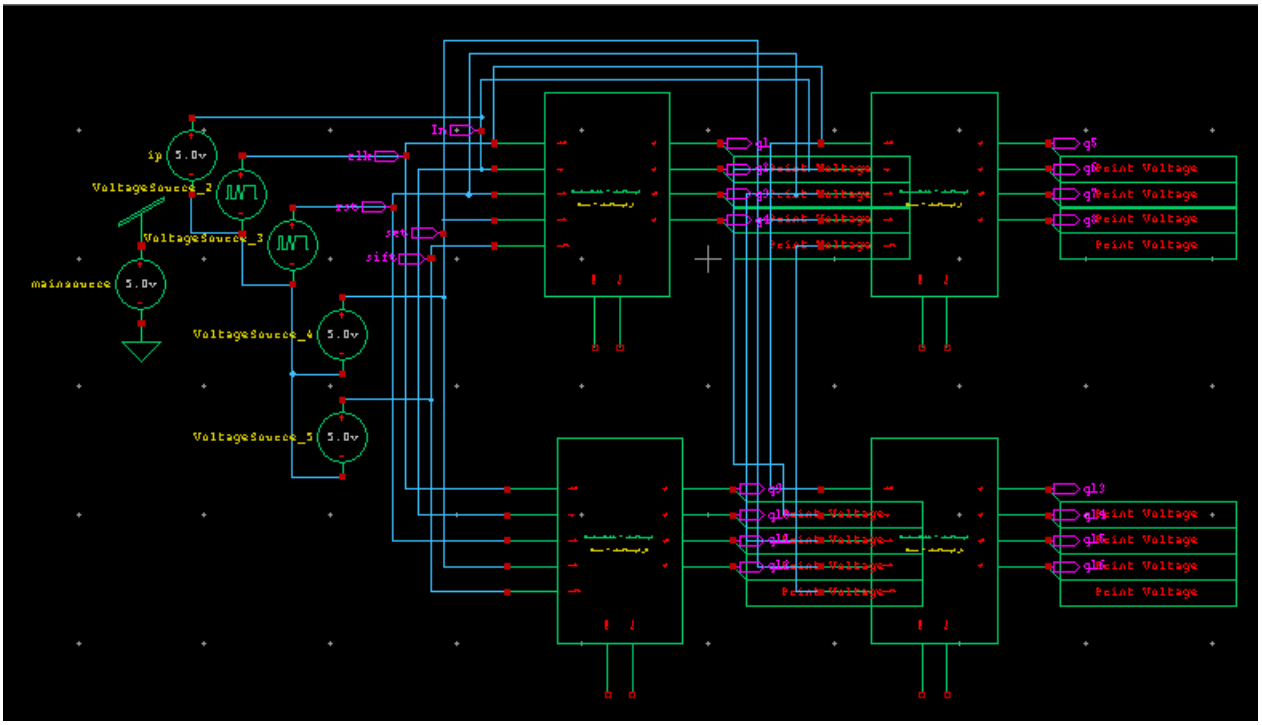

Fig8.10 Fin-FET based parallel to Serial block

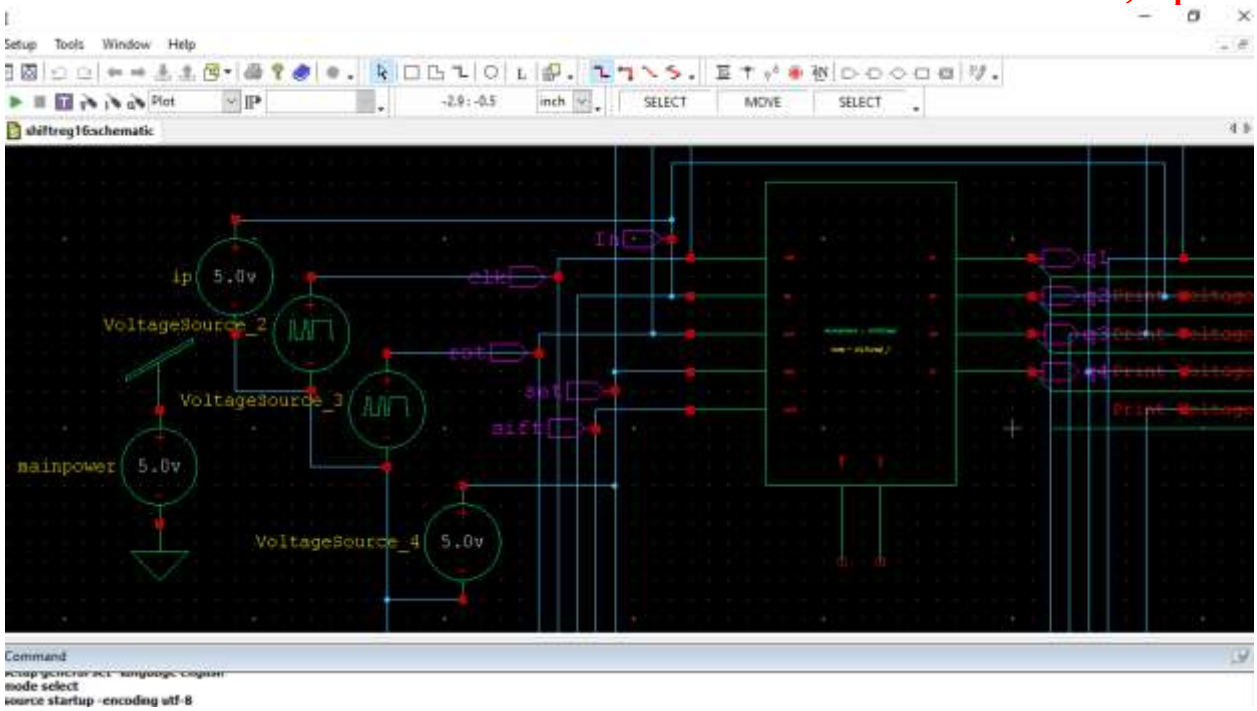

Fig 8.11 Fin-FET based multiplexer design

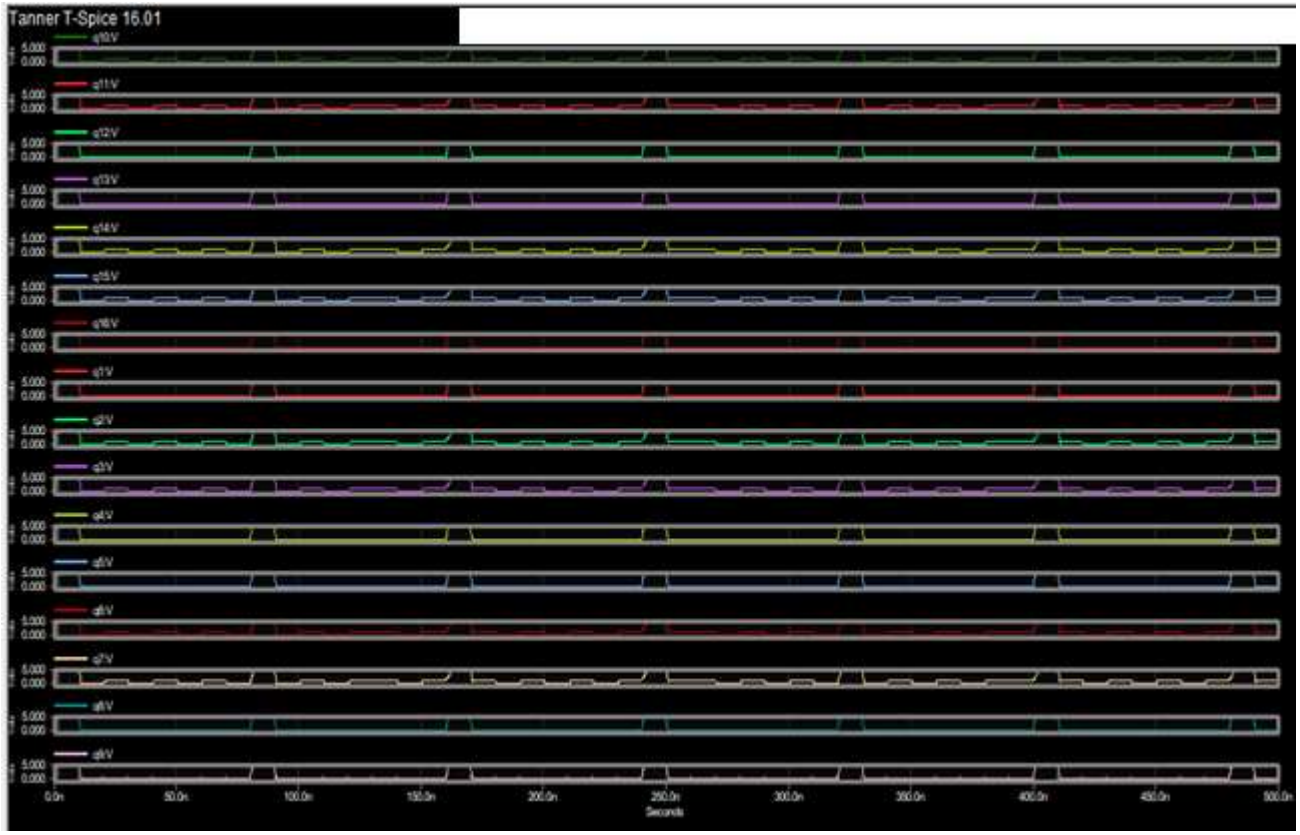

Fig8.12 Simulation result of parallel to serial conversion

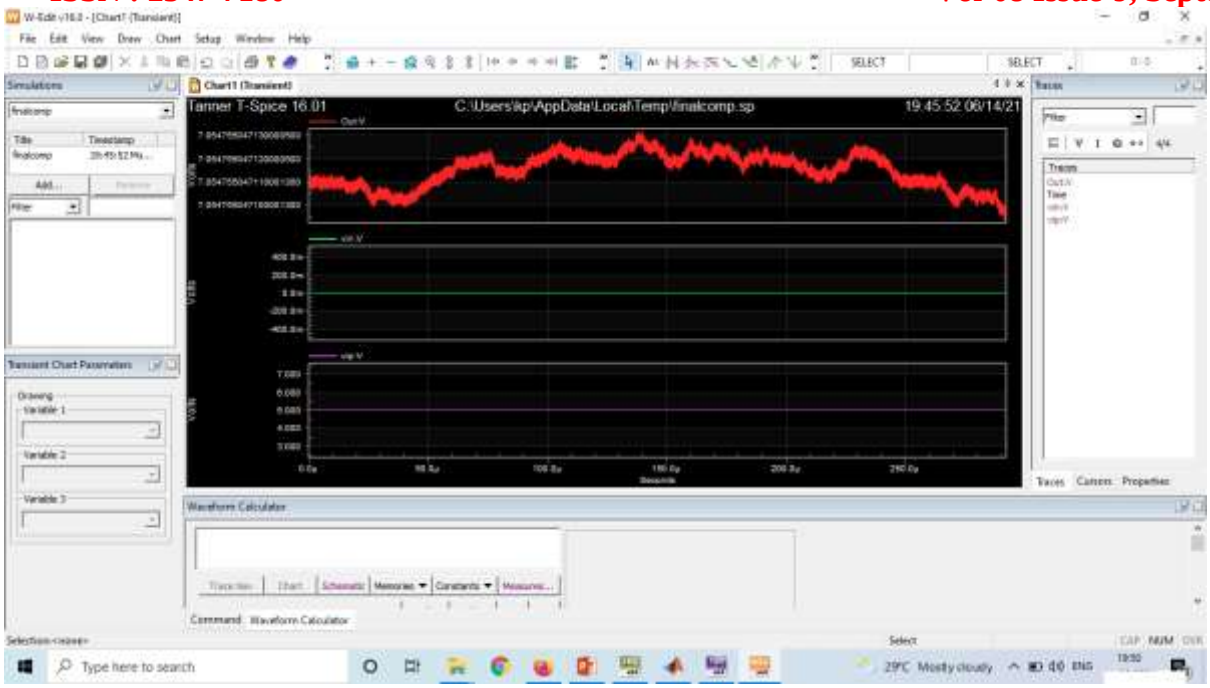

Fig:8.13 simulation output of mux with one combination

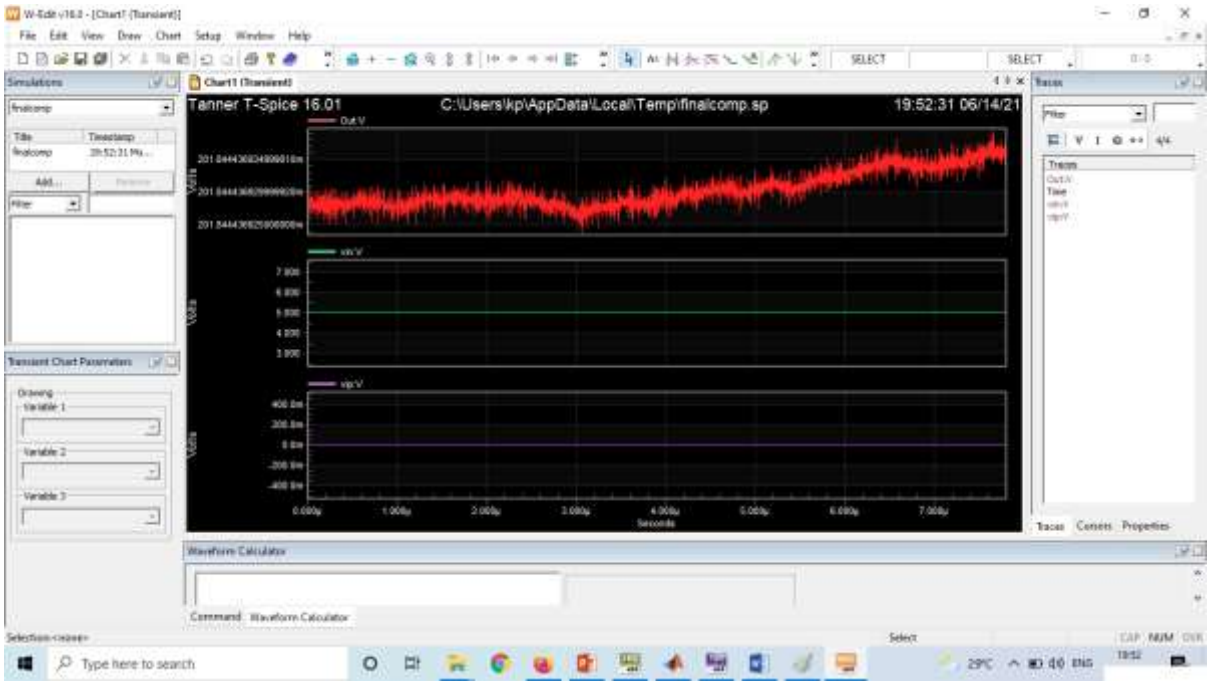

Fig:8.14 simulation output of mux with second combination

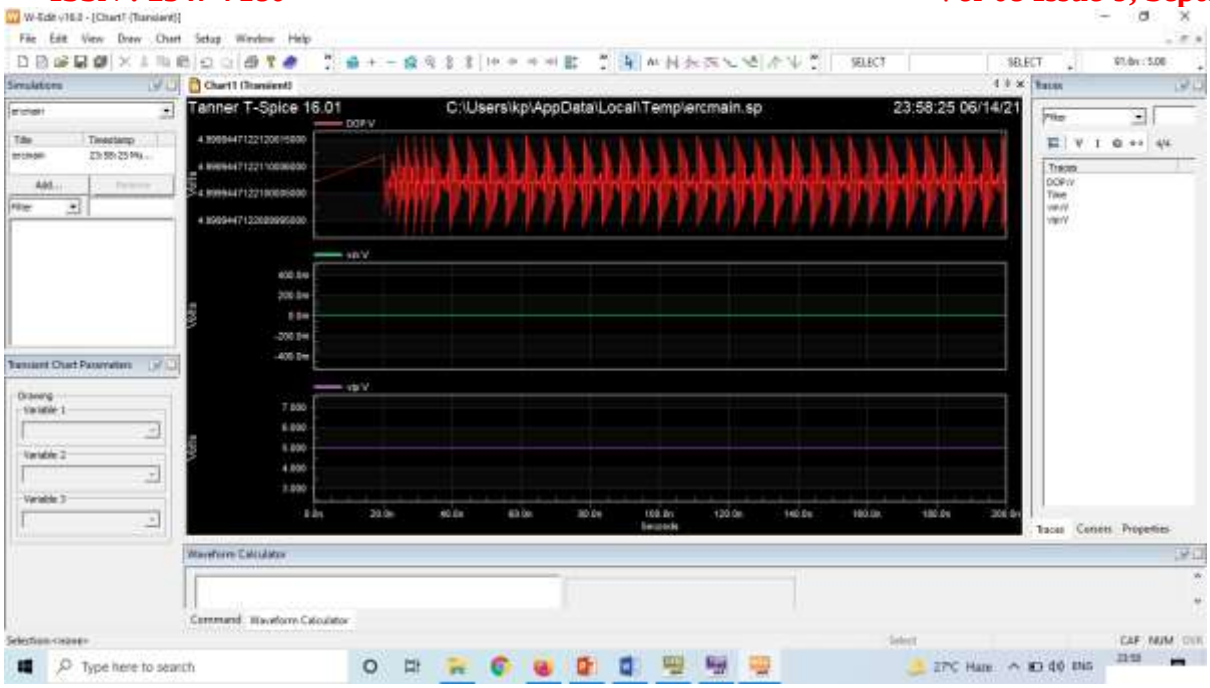

Fig:8.15 simulation output of mux with third combination

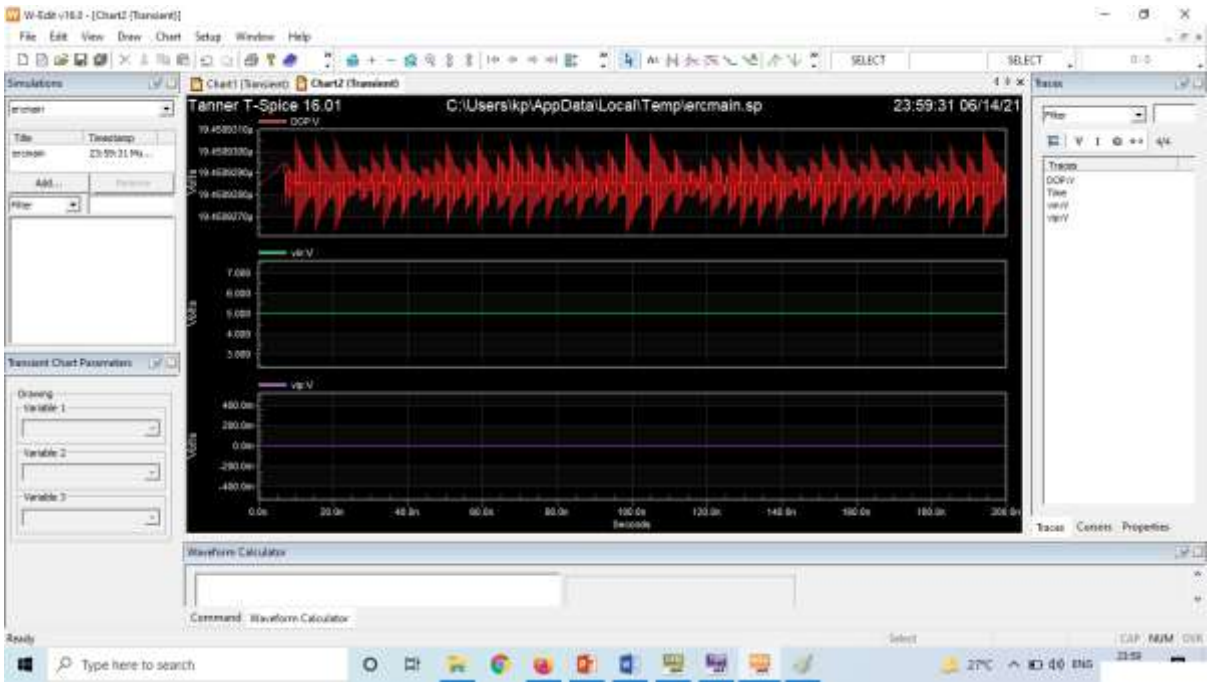

Fig:8.16 simulation output of mux with fourth combination

CONCLUSION:

FinFET not only has superior performance over bulk silicon MOSFET, but is primed to take over bulk silicon MOSFET as the dominant transistor choice for sub-7 nm. In this research, presentd a methodology for synthesizing logic circuits using independent-gate FinFETs, which leads to reduction in number of transistors (and chip area) needed to implement circuits. The methodology is based on the existing MOSFET circuit synthesis methodology and can be readily adapted for independent-gate FinFETs by making minor modifications. Simulation results show that compared to other logic implementations, FinFET logic circuits achieve significant area and power reduction without voltage or transistor scaling, even though they suffer greatly in circuit speed.

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